ATLAS Internal Note
October 99

Tile-Cal ROD functional specifications

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1 Introduction

ROD modules are place at the end of the Front-End electronic chain. Their general functionalities can be found in [1] and are summarized below:

1. **Raw Data gathering from first level de-randomizers at the L1A event rate** $100Khz$.
2. **Standard ATLAS data format**. TTC signals will be present at each module providing ROD_L1ID, ROD_BCID and trigger type.
3. **Synchronism Trigger Tasks** The ROD must check that the owner BCID and L1ID numbers match with the ones received from the FE. If a mismatch is detected, a flag must be set with some error code.
4. **Event data must be sent to ROB through the standard ATLAS readout links** at the L1A event rate.
5. **Provide a ROD busy signal** in order to stop L1A generation. A global OR of the busy ROD's per sub-detector has to be provided to the CTP.
6. **Local Monitoring of the data flow** during a run without introducing dead-time or additional latency in the main DAQ data flow.

Beside these, **Tile-Cal RODs** will the have the following functionality with respect to **data processing**:

- **Provide energy, timing and pile up estimation to the next level by optimal sample filtering**
- **Possibly to pass raw data** without processing when it be advisable (pile-up, high energy events)

We assume a one to one correspondence between the ROB and ROD, but a multiple correspondence will be used between FE motherboards and the ROD in order to obtain a higher degree of data multiplexing.

2 Front End Readout

Tile-Cal detector is divided in 64 sectors for the barrel and the extended barrel, giving a total of 256 super-drawers, and approximately 10000 electronic channels. For each channel, the digitizing system will provide a set of 5 to 7 samples of 10 or 12 bits (not decided yet), separated by the BC period (25ns). The expected raw bandwidths for the barrel and extended at $100KHz$ L1A are shown at Table 1

However, the event data packets will have control and status bits between the data stream. For 10 bit samples, we can fit three of them in a 32 bit word leaving space for some error detection bits. The format for 5 or 7 samples per PMT is shown in Table 2. For data samples of 12 bits it is not possible to have a so good matching of the samples in 32 bit words, and only 2 PMT samples can be fitted in the 32 bits, leaving 6 bits unused. The bandwidth required in any of the above cases is presented in Table 4 for the barrel and the extended. Therefore the Tile-Cal event is break up in a 17% of headers and a 83% of data. To keep

	$\frac{1}{2}$ *Barrel Module*				1 *Extended Module*			
PMTs	46				31			
CELLs	23				14			
Bits Per Sample	12	12	10	10	12	12	10	10
Samples	7	5	5	7	7	5	5	7
BW Mbits/s	386	276	230	322	235	168	140	196

Table 1: *Raw data bandwidths.*

Control Flag	*DIGITIZER Control/Status Bits and BCID LVL1*			
Data Flag	Parity Flag	$\text{Sample}_0\text{-PMT}_i$	$\text{Sample}_0\text{-PMT}_{i+1}$	$\text{Sample}_0\text{-PMT}_{i+2}$
...	...	...	...	...
Data Flag	Parity Flag	$\text{Sample}_6\text{-PMT}_i$	$\text{Sample}_6\text{-PMT}_{i+1}$	$\text{Sample}_6\text{-PMT}_{i+2}$
Control Flag	*Vertical Parity by bit*			

Table 2: *FE link data packet format with 10bit samples.*

the number of RODs low, a mapping of 4 super-drawers to 1 ROD could be possible without exceeding the Read Out Link bandwidth to ROBs ($1.6\frac{Gbit}{sec}$). The FE Link technology is not decided but it seems that the protocol will follow that of S-Link.

3 ROD schematic block diagram and functionalities

The basic data processing at ROD will consist in **correcting data according to calibration tables, bunch crossing identification and best energy deposition estimate for each cell**. Besides this data processing, ROD must give the data a common format defined for the whole ATLAS detector, send and receive the necessary control signals, including TTC, and provide a mechanism for local control and monitoring. ROD module schematic block diagram is shown in Figure 1.

3.1 Front End data reading

As mentioned before, **each ROD module will gather data from 4 superdrawer, 184 channels, in parallel**. Data coming from the detector digitizers will be read through optical fibers and stored in a FIFO memory. The first operation to be done on data is the extraction of the header which contains the BCID number. This information will be checked against that obtained from the TTC signals. If a mismatch is encountered, an error flag should be asserted to disable ROD from processing that data.

3.2 Energy estimation

The **Shape Waveform and Energy Threshold Analysis** will guide the subsequent processing of the data read. This module would be able to detect the presence of pile up or high energy events in the data, the absence of data (empty event) or a good event. In each one of these cases, the processing differs. The module could be implemented in a hardware device, such as an FPGA, where a shape checking and data comparison algorithm could be run. In the case of pile-up detection, if the energy is above a programmable threshold or if

Control Flag	*DIGITIZER Control/Status Bits and BCID LVL1*			
Data Flag	Parity Flag	*SPARE bits*	Sample_0-PMT_i	Sample_0-PMT_{i+1}
...	...	...	...	...
Data Flag	Parity Flag	*SPARE bits*	Sample_6-PMT_i	Sample_6-PMT_{i+1}
Control Flag	*Vertical Parity by bit*			

Table 3: *FE link data packet format with 12bit samples.*

	$\frac{1}{2}$ *Barrel Module*				1 *Extended Module*			
NoPMT	46				31			
Bits Per Sample	12	12	10	10	12	12	10	10
Samples	7	5	5	7	7	5	5	7
Packet Size	36	28	28	36	36	28	28	36
NoPackets	23	23	16	16	16	16	11	11
BW Mbits/s	632	492	342	440	440	342	235	275
$\frac{Header}{Data}$	$\frac{42}{58}$	$\frac{46}{54}$	$\frac{36}{54}$	$\frac{30}{70}$	$\frac{43}{57}$	$\frac{48}{52}$	$\frac{37}{63}$	$\frac{31}{69}$

Table 4: *Expected formatted data bandwidths.*

an empty event is detected, ROD could skip the data processing and download the complete set of pulse samples to the next trigger level, where further data analysis could be done.

A pulse will be considered good when only one event is detected in the actual trigger. In that case, for each set of samples per channel, **ROD should obtain a value for the energy deposited in each cell and a timing estimation**. To compute these values it will be necessary to determine the timing and amplitude information of the data set by means of **optimal filtering**. This technique implies the knowledge of the canonical function of the complete electronic chain and the assumption of the linearity of the system in the whole dynamic range. The output waveform from the analog TileCal-Electronics chain is shown at Figure 2. In case we do not have a good event the results provided by the optimal filter could be a nonsense value, as could happen in the case of *pile-up or with minimum bias* events. *Optimal filter* coefficients should be loaded before operation in a *Look Up Table* inside the processor memory by means of the control system described below.

Even main ROD data processing is that of the energy and timing estimations, there could be the possibility of performing a trigger tower calculation. Nevertheless, further studies would be necessary with this respect to assure ROD will provide the required confidence factor to the results.

3.3 ATLAS formatting

With the results of the data processing, ROD would assemble a data packet which will follow ATLAS common format. This format make several assumptions on the link between RODs and ROBs, these are:

- All words are 32 bit
- The Read Out Link (ROL) is able to distinguish between data and control words.
- All fragments begin and end with a control word.
- A control word is only used at the beginning an end of the fragment.

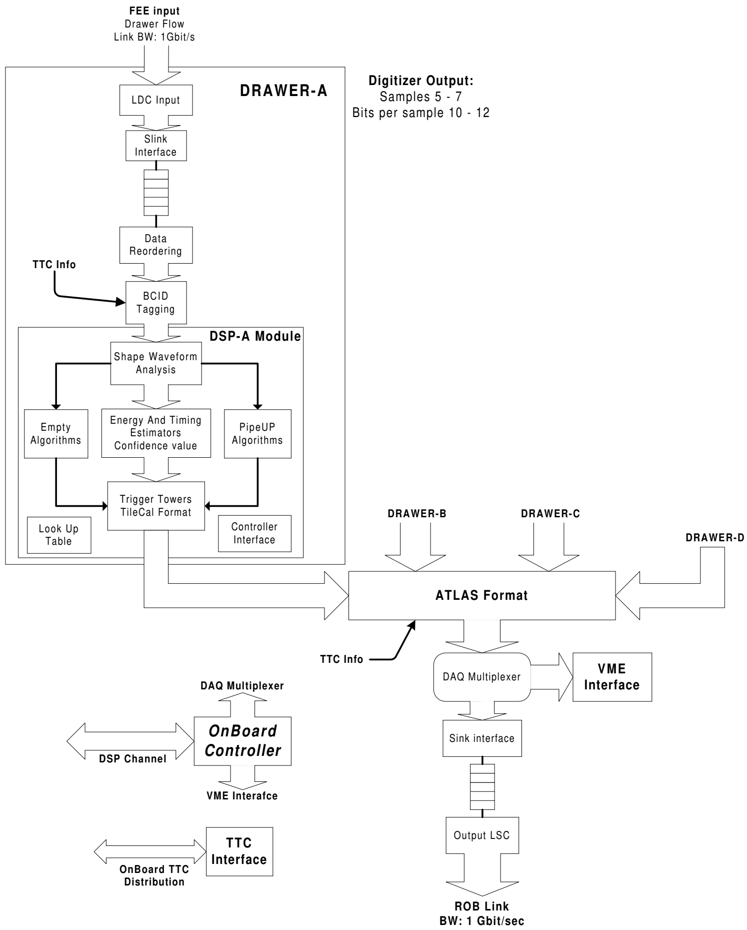

Figure 1: *Tile-Cal ROD Schematic Arquitecture.*

- The fragment size is variable and not limited.
- Empty fragments may be sent.
- Any words of unknown content should be set to hex 00000000.

The current format to be used for ROL is showed at Figure 3. Lets explain briefly the meaning of each field:

- *Begin of Fragment*: Constant word which defines the begin of the fragment
- *Start of Header Marker*: Required by DAQ to identify ROB fragments
- *Header Size*: Number of words in the header (do we need a variable size header?)
- *Format Version Number*: Declares the particular format used in the fragment
- *Offset to Status Block*: Word count from the start of the fragment to the beginning of the status block
- *Source_ID*: Identifies each ROD
- *ROD_L1ID*: 24bit number which identifies the event

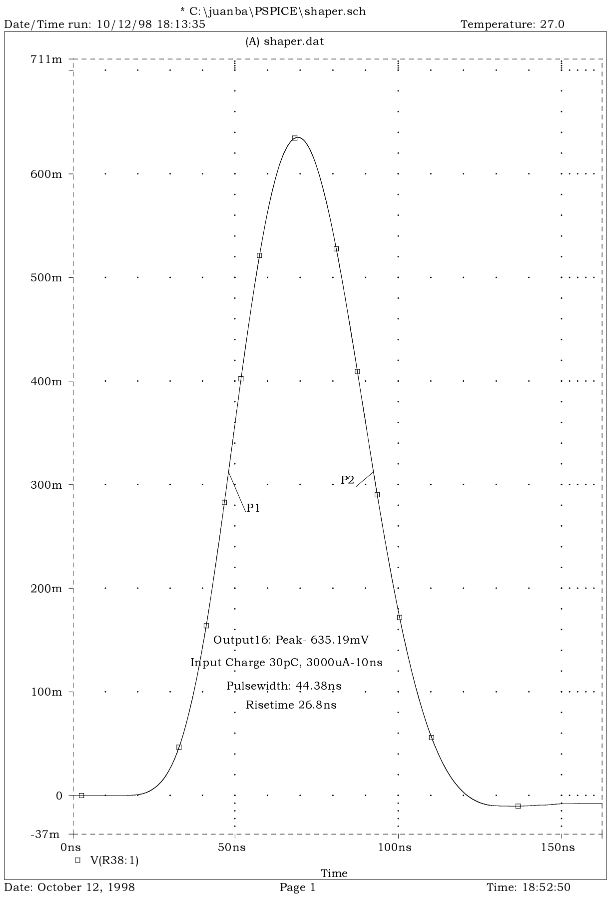

Figure 2: *Tile-Cal Shaper Output Waveform.*

- *ROD_BCID*: 12bit number which identifies the bunch crossing
- *Level 1 trigger type*: Sent by the TTC. Defines the trigger type
- *Detector Specific Event Type* : Required by DAQ and filled at ROB level. Defines the event type from the point of view of the detector.
- *Data and status words*: Present event data and status (error, fake event, calibration, physics, ...)
- *Status summary and Status Word* : 16bit words. The first summarizes the content of the status set (to be defined); the second is a count of the number of status words
- *No. of Data Words*: Data words counter
- *End of Fragment*: Constant word that defines the end of the fragment

Assuming a maximum of 16 bit for the energy and timing estimations, each channel information would fit in a 32 bit word, so for the four super-drawers the total packet size will be:

Word Number	Word Content	Word Type
0	Begin Of Block 0xB0B0 RRRR	Control
1	Start of Header Maker 0xEEEEEEEE	Data
2	Format Version Number	Data
3	Header Size	Data
4	Offset of Status Block	Data
5	SOURCE_ID	Data
6	ROD_L1ID	Data
7	ROD_BCID	Data
8	Level 1 Trigger Type	Data
9	Detector Specific Event Type	Data
..	Data And Status Words	Data
	This area consists of a block of N status words and a block of M Data words. The position of the block of Status words is given by the **Offset to Status Block** in word 4	
M+N+10	Data And Status Words	Data
M+N+11	Status Summary | No of Status words N	Data
M+N+12	No of Data Words M	Data
M+N+13	Begin Of Block 0xE0B0 RRRR	Control

Figure 3: *ATLAS Event Format.*

3.4 DAQ Multiplexer

ROD must provide an access to data different to normal to perform monitoring on data. The DAQ multiplexer will direct data flow to ROBs or to the VME bus to accomplish with this functionality. There could be several modes of operation:

- if ROB Link is enabled, **spy some percentage** $(1\% - 5\%)$ **of the ATLAS DAQ data flow using the VME bus** .
- if ROB Link is disabled, **spy the complete data flow at a reasonable rate using VME bus** $(100Hz - 1KHz)$. Block and single transfer capabilities will be therefore needed.
- **Monitor ROD_BUSY signal**, using a VME interrupt.
- For each ROD module, monitor the status of the different components in the ROD architecture, *Minimum Bias and Pile-Up* noise.

3.5 On-Board Controller

This module will **control the operation of the whole ROD module**. Its main tasks are:

Word Type	*Number of Words*
Header	10
Data	124(Extended)-128(Barrel)
Status	X(Not Defined Yet)
Footer	3
Total	(137-197) + X words

Table 5: *OutPut Event Size.*

- **Execute the command received through VME bus from the user** (run programs, load LUTs, calibration tables, etc.)
- **Control the data flow** either Monitoring or Normal data taking
- **Manage the ROD_BUSY signal**. ROD must be able to stop LVL1 trigger generation, asserting the ROD_BUSY signal, under several conditions:
  - XOFF return signal from ROB
  - Input buffer from Front End full
  - Output buffer to ROB full

It has also to provide the following features:

- ROD_BUSY and its activating conditions must be reset-able and maskable by software
- ROD_BUSY state produced by a ROB XOFF must be recovered by the ROB XON
- Statistic monitoring of ROD_BUSY, including ROD_ID and BUSY condition

3.6 TTC Interface

ROD receives all the standard TTC signals, including ROD_L1ID (event number, 24 bits), ROD_BCID (BC number, 12 bits) and trigger type. A distributing systems of the TTC signals is required and a crate level. There could be two basic approaches:

- **To have a VME TTC module with the TTCrx chip, distributing the signals along the ROD crate using an internal bus system (P2 connector?)**. This is cheap but it is not fault tolerant and the bus must provide a performance according to the de-randomizing output rate ($100KHz$).
- **To have a TTCrx chip for each ROD module**. This is an expensive solution but highly fault tolerant. The TTC receiver could be a mezzanine card plugged on ROD-Module mother board.

3.7 Read Out Link

The Read Out Link is used to transmit the data from RODs to ROB at the L1A rate. The T/DAQ group will provide the specifications of this link. In order not to saturate the ROL bandwidth ($1.6\frac{Gbit}{sec}$), ROD algorithms must produce an output flow below this limit. Keeping a 15% safety factor on the ROB link, a single ROD should not produce more than $1.36\frac{Gbits}{sec}$. With the $\frac{4}{1}$ mapping, the total amount of data to be sent is of $197+X$

32 bit-words, where X is the number of status words. With the limit imposed, the maximum number of status words could be of 259; that is, it could be possible to have one status word per channel to signal errors or other kind of information needed. In that case, the output rate would be of $1.14\frac{Gbits}{sec}$. The technology and the protocol of this link is not yet decided and should be agreed with the whole ATLAS collaboration.

4 ROD Control

From the users point of view, ROD should provide the general functionalities which will allow them to control the whole system. In particular, but not only, the users should be able to:

- **Download the ROD software to each ROD module**: DSP Code, Lookup tables, optimal filtering parameters, and Calibration tables, etc.
- **Masking, Enabling and Reset of each stage in the RODs algorithms** (Empty algorithms, Energy Algorithms, etc..).
- **Start the calibration runs**, analyze the data and extract the optimal filtering algorithms. It is **desirable to have an independent trigger management without the general ATLAS DAQ trigger**.

In such a way, an environment to make tests and check the different components of the ROD system is provided.

5 Summary

- Number of RODs: 64
- Number of super-drawers per ROD: 4
- FE Link bandwidth: $1.6\frac{Gbits}{sec}$
  - Maximum expected BW Barrel: $632\frac{Gbits}{sec}$
  - Maximum expected BW Extended: $385\frac{Gbits}{sec}$
  - FE Link technology: probably optical
  - FE Link protocol: S-LINK
  - FE Link format: see table 2
- Data processing:
  - BCID checking and error detection
  - Data processing:
  - Energy, timing and pile-up estimation
  - Data formatting according to ATLAS format
- ROL Link bandwidth: $1.6\frac{Gbits}{sec}$
  - Expected BW: $1.14\frac{Gbits}{sec}$

- ROL Link protocol: (to be agreed with the ATLAS collaboration)
- ROL Link technology: (to be agreed with the ATLAS collaboration)
- ROL Link format: see table 3

References [1] ATLAS T/DAQ Steering Group. Front End requirements document.