The Tile Calorimeter read-out is based on a fast digital sampling of a shape waveform. Commercial ADCs (Analog Devices ADC9050@ 40MHx) are used for sampling the signal. Two shapes of the same signal are digitized, one for low and another one for high gain (amplified a factor of 64). The inputs of the RoD are signals with 7 or 9 samples and high or low gain, except if a calibration mode is in, in which case both gain signals are sent to the RoD.

For the present analysis a normal operation mode with 9 samples signals were chosen. A header before the data indicates if the signal from one PMT channel was sent in high or low gain.

OPIMAL FILTERING ALGORITHM

Optimal Filtering algorithms allows a good reconstruction of timing and amplitude from calorimeters multiply sampled signals minimizing the noise.

The advantage of this method is the reduced sensitivity to channel-to-channel variations.

Linear combinations of the samples are used in order to recover the signal parameters, sampled shaped signals minimizing the noise.

The Flat Filtering algorithm is a very fast and simple method to estimate the energy adding all signal samples.

The Implementation of Flat Filtering on the DSP is equall to the implementation on a floating point processor but using look-up tables in order to reduce processing time.

Data from the FEB are received with a S-link ODIN link destination card (LDC) whose firmware was modified to cope with the TileCal FEB interface link custom protocol based on on-chip HDMP1032. This LDC is mounted in a transition module in the rear part of the back-beam region of the calorimeters and houses up to 24 pairs of PMTs.

The ATLAS Hadron Tile Calorimeter (TileCal) Read-out Driver (RoD) modules are 9U VME cards which are in charge of reading and computing data from the TileCal front end electronics boards (FEB). The RoD motherboard has four mezzanine Processing Units (PU) cards, with a Digital Signal Processor (DSP) implemented with signal energy and time reconstruction algorithms. The board also contains several FPGA ABICS for input/output data management and VME protocol control. The cards are inserted in standard VME crates. They receive data through optical fibres from the FEB and send them to a Transition Module (TM) installed at the back of the VME crate.

During the summer 2003, a prototype design of the RoD for the Tile Hadronic Calorimeter of ATLAS, the RoD Demonstrator board, was integrated in a parallel data acquisition system for the TileCal beam test. The standard data acquisition system was used for the off-line data taking using RoD Emulators, while the RoD Demo was debuged and tested in parallel to data taking.

The beam test was performed in the north area, Prévessin, at CERN. Two central barrel modules and two extended barrel modules were targeted by the beam line from the SPS. Each half-barrel module and each extended barrel module has a super-drawer which contains all the front end and digitizing electronics. Our aim was to read one super-drawer (FEB) with one RoD Demo and one Processing Unit and study its performance. An industrial rack PC with an S-link to PCI card was used to store the data and used as a RoD (Read-out Buffer) Emulator.

In ATLAS, the calorimeters are divided into 64 modules. The whole calorimeter covers the region of  $-1.7 < \eta < 1.7$ in several directions in $\phi$.

During the beam test the four modules are on a mobile table which allowed to scan them in several directions in $\eta$.

Concerning the Timing and Trigger Control (TTC) information, there is a PMC board called TTCp mounted in the SBC. This card has basically an optical receiver, a STC chip to decode TTC multiple purposes information and a PCI bridge. The RoD controller reads continuously the TTC information when it is available and sends it through its VME bridge chip to trigger the slave RoD Demo module.

During the beam test the modules were on a mobile table which allowed to scan them in several directions in $\eta$. During the summer 2003, a prototype design of the RoD for the Tile Hadronic Calorimeter of ATLAS, the RoD Demonstrator board, was integrated in a parallel data acquisition system for the TileCal beam test. The standard data acquisition system was used for the off-line data taking using RoD Emulators, while the RoD Demo was debuged and tested in parallel to data taking.

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