Results from the 1999 H8 beam tests of SCT prototypes

January 2000

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Abstract

This note summarizes the results from three independent analyses of the August-September 1999 test beam data, collected in H8 at CERN. Three half-modules, equipped with the principal candidates for the SCT Front End electronics, have been tested. Results are presented on efficiency and noise. In addition, a study of the characteristics of the shaper is reported.

1 Introduction

Beam tests provide an opportunity to verify the functioning of detector prototypes in a realistic environment. The main objective of the August-September beam test was to study the characteristics of the various existing types of SCT Front End readout chips.

To this end, three single sided prototypes of SCT binary modules were tested, each of them populated with a different type of binary Front End electronics. In all cases, the chips were fully bonded to 12 cm of 325 μm thick, barrel type, p^+n Hamamatsu detectors. None of the modules had been subject to irradiation. The CAFE/ABC module was built at Lawrence Berkeley National Laboratory, both ABCD modules at the University of Geneva. Below, the modules under test are listed specifying the FE readout chips and the hybrid.

- ABC1 : 6 CAFE/P + ABC FE chips on LBL Beryllia hybrid
- CGNT1: 6 ABCD2NT chips on Oslo Alumina hybrid
- CGT1 : 6 ABCD2T chips on Oslo Alumina hybrid

ABCD2T denotes the ABCD chip version equipped with trim DACs which correct the channel to channel gain and offset variations, whereas ABCD2NT refers to the non-trimmable version. Detailed descriptions of the CAFE/P, ABC and ABCD Front End chips can be found in references [1, 2, 3], respectively.

This paper summarizes the main results of the August-September beam test. Section two contains a brief discussion of the setup and the operation of the modules during the beam test. Then, section three reports the results on efficiency and noise from the three independent analyses of the test beam data. Section four studies in more detail timing effects related to the shaper characteristics of the modules. Finally, section five contains a summary of all results.

For a more extensive introduction to ATLAS and the Semiconductor Tracker, the reader is referred to the Inner Detector Technical Design Report [4] or the ATLAS and SCT web pages [5, 6]. More information on the test beam can be found on the test beam web pages [7] or in previous internal notes [8, 9, 10].

2 Setup and experimental conditions

The H8 SCT test beam setup comprises a number of detectors providing additional information. Four pairs of telescope planes are installed in the beam. The perpendicular silicon strip detectors with analogue readout enable precise three-dimensional track reconstruction. Further, the fact that the SPS beam in H8 is asynchronous introduces a 25 ns random phase of the trigger with respect to the 40 MHz system clock. This trigger phase is measured using a scintillator detector and a Caen V488 TDC.

For control and readout of the binary modules the test DAQ system [12] is used, consisting of CLOAC, SLOG and MuSTARD VME modules. The binary data are stored together with the information from the telescopes and the TDC in the RD13 format. The raw data are processed off line into DSTs, available at [11].

In the 1999 beam tests, a fourth binary module - CG3 - was introduced in the beam. It served as a reference and was kept at a fixed bias voltage and threshold throughout the beam test ($V_{\rm bias}$ = 80 V and Thr = 200 mV). This permitted the relative efficiency between the fixed efficiency reference module and the modules under test to be measured under all conditions, resulting in very low residual inefficiencies.

The run conditions are largely determined by the configuration of the Front End chips. Both the ABC and ABCD FE chips provide binary hit information from the triggered, central time bin, as well as from the previous and next time bins. All data was taken in Anyhit ($1XX|X1X|XX1$) data compression mode, i.e. hit information was accepted whenever a hit was found in either of the three time bins. More realistic compression modes like Level (X1X) or Edge (01X) compression accept a subset of these data. Therefore, hit information in both compression modes can be obtained from the Anyhit data off line.

Moreover, both chips are equipped with an edge sensing circuit that on detection of a low to high transition in its input data outputs a pulse of duration 1 clock cycle, irrespective of the length of the incoming pulse. Thus, when the edge sensing circuit is activated, only one "1" is written into the pipeline for every hit detected.

The data consists of four thresholds scans taken with the edge sensing circuit switched ON/OFF and at two different detector bias voltages : $V_{\rm bias}$ = 80 V and $V_{\rm bias}$ = 240 V.

The detector bias voltage primarily affects the charge collection time and thus the input pulse shape. Assuming a uniform field in the Silicon detectors $E_{Si} = V_{bias}/d$ one can estimate the total charge collection time as a function of detector bias voltage:

$$T = \frac{d^2}{\mu V_{bias}} \tag{1}$$

where d is the thickness of the silicon and μ is the mobility of the charge carriers. For 325 μm thick p^+n detectors one expects total charge collection times of 27 ns and 9 ns for 80 V and 240 V respectively.

For the three modules two calibrations were available, one provided by the home institutes and one done in H8 immediately after the beam test. The points of all calibrations in figure 1 are the average of the 50% efficiency points of all channels, obtained by a fit to the individual response curves.

The calibrations are in good agreement for ABC1 and CGT1, but give different results for CGNT1. In order to be able to compare results, all three analyses use the same calibration, calculated directly from a three-parameter fit of the in situ points without any offset applied. Also note the highly non-linear response of the CAFE/P amplifier.

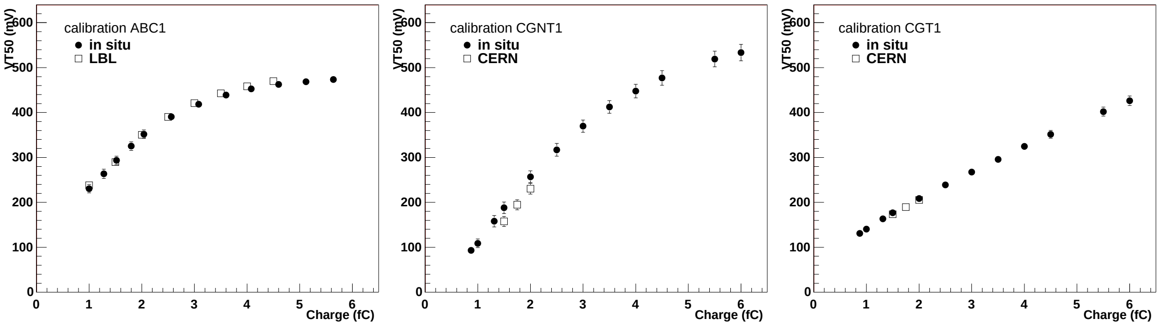


Figure 1: *Comparison of in situ and home institute calibrations, a) ABC1, b) CGNT1 c) CGT1*

It was found that at low thresholds (up to $\simeq 0.9$ fC) the ABC1 module was not functioning stably.

As an illustration, figure 2 shows hits (black dots) versus channel number and event number for the cleanly operating reference module (on the left) and for ABC1 at 0.9 fC (on the right). The reference module has almost all its hits in the beam region, roughly from channel 450 to 500. The gaps correspond to 30 noise events taken after every spill. In the ABC1 module, on the other hand, one observes horizontal bands corresponding to events with very high noise occupancy. The high occupancy at low threshold may lead to event size problems in the DAQ and off line analysis. Therefore, the threshold scans are limited to thresholds above ~ 0.8 fC and runs showing signs of instability are rejected.

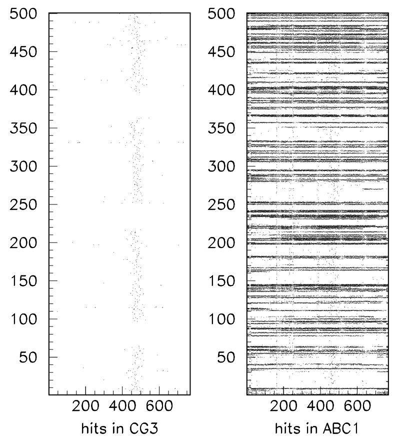


Figure 2: *Hit channels versus event number for CG3 at 200 mV (left) and ABC1 at 0.9 fC (right)*

3 Measurements of efficiency and noise

This section describes the conventional test beam analysis method and presents efficiency and noise results from two analyses. In addition, an alternate method using only information from the binary modules is discussed.

3.1 Analysis using beam telescopes

The conventional test beam analysis compares the response of the binary modules to tracks reconstructed using the information from the beam telescopes. The efficiency is evaluated by extrapolating the telescope track[1] to the plane of the module under test. Only the central, triggered time bin is considered[2]. If a hit is found within 100 μm of the track, the event is considered efficient. Noise is evaluated directly from the noise events taken after every spill.

The TDC measures the relative timing of the charge deposition moment (trigger) and the sampling moment (system clock), which has a strong effect on efficiency, as shown in figures 8 and 9. In order to evaluate the modules in circumstances similar to the synchronous beam at LHC, a narrow TDC window is chosen separately at each threshold such that the efficiency is maximal. Events falling outside this window are not considered in the determination of the efficiency.

Finally, an irreducible inefficiency of approximately 2% was found. The two conventional analyses effectively removed this inefficiency by requiring the reference module to be efficient.

Figure 3 summarizes efficiency and noise occupancy results as a function of threshold, accepting all channels in the analysis.

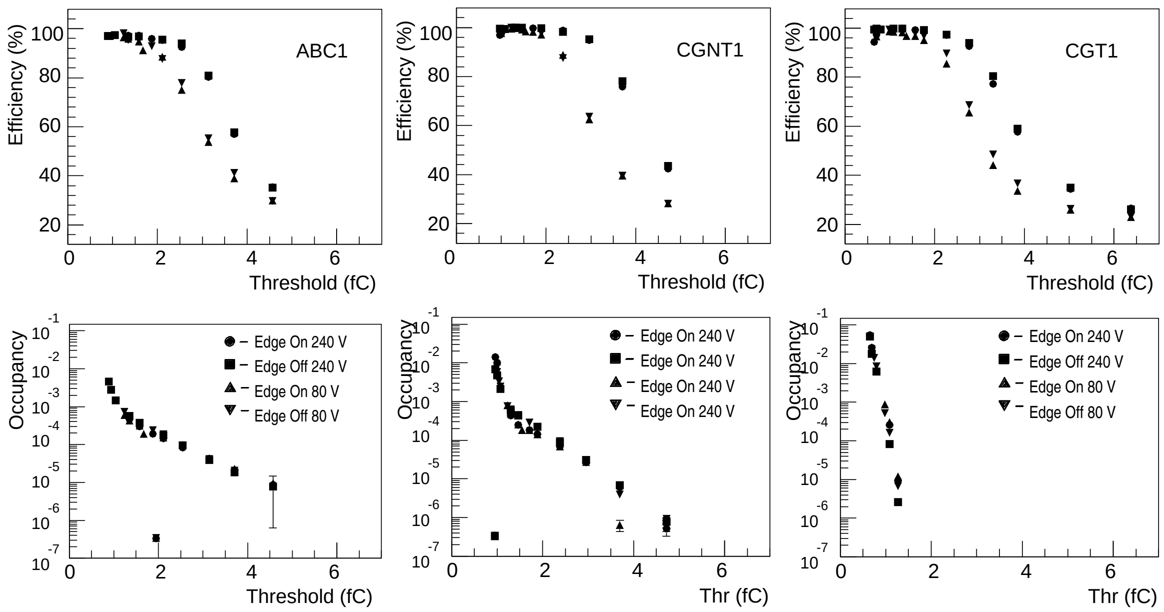


Figure 3: *Efficiency and Noise occupancy versus threshold, including all channels*

[1]The analysis is limited to events with one reconstructed track in order to avoid ambiguities.

[2]Off line, the data taken in $1XX|X1X|XX1$ compression mode is reduced to $X1X$ compression mode

The second analysis rejects all bad channels[3] in order not to be influenced by bonding errors or detector defects. In addition, the efficiencies are obtained from a fit of a complementary error function to the efficiency versus TDC distribution (these distributions are discussed in the timing study).

Figure 4 shows the results on efficiency and noise after bad channel rejection. In two modules, ABC1 and CGNT1, the noise tail at high thresholds is drastically reduced by rejecting bad channels (80 and 11 channels respectively). In the CGT1 module no bad channels were found. The noise occupancy as a function of threshold is now described reasonably well by a Gaussian, apart from deviations at the 10^{-4} level for the ABC1 module.

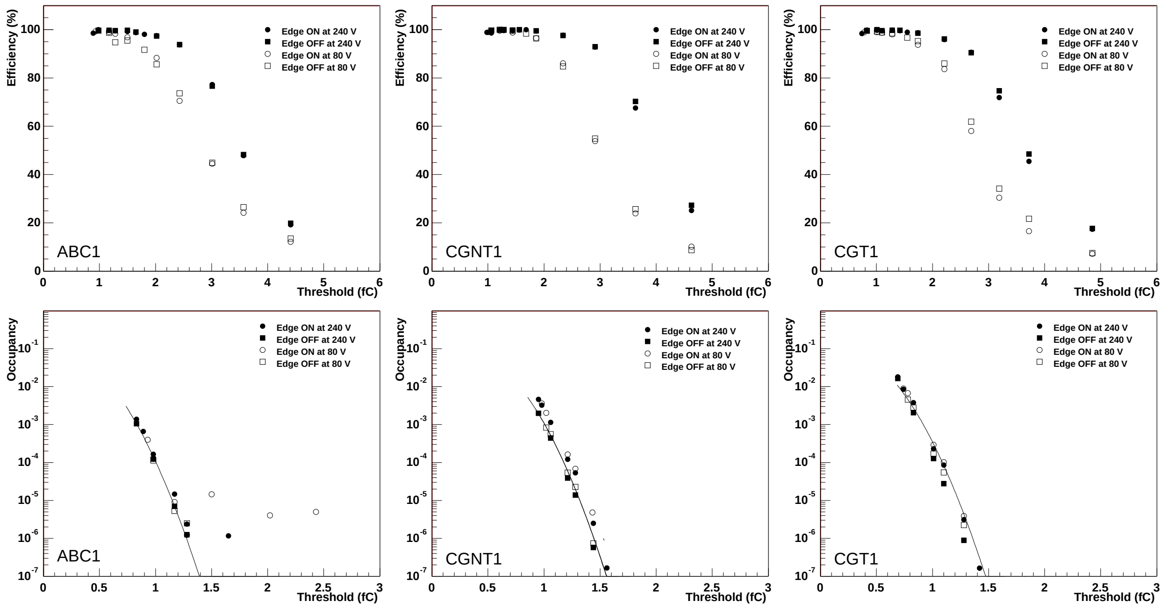


Figure 4: *Efficiency and Noise occupancy versus threshold, after bad channel rejection*

At the baseline ATLAS operation threshold of 1 fC[4], all three modules provide high efficiencies: $> 99\%$ for 240 V and $> 98\%$ for 80 V and low noise occupancy ($< 10^{-4}$). Detailed efficiency and noise figures from the three analyses can be found in the summary of results concluding this note.

Except for a slight degradation of the efficiency for very low thresholds (Thr ~ 0.8 fC) in the case of edge On, there is no noticeable difference between edge ON and edge OFF data.

On the other hand, the detector bias voltage is seen to have a very profound effect on the efficiency curves. The much lower efficiency for the 80 V scans is probably due

[3] A channel is considered bad when its occupancy is a factor four different from the chip average

[4] For CGNT1 the optimum efficiency and noise are achieved around $1.2 - 1.3 fC$. All numbers are quoted for this point

to a ballistic deficit in the shaper[5], regarding the expected large charge collection time at 80 V bias with respect to the shaper peaking time. The timing study in section 4 discusses this question in more detail.

3.2 Monte Carlo

The efficiency results at 240 V detector bias are in good agreement with the S-curve of figure 5 obtained by a Monte Carlo simulation. Input charges to the Front End electronics are generated according to a Landau dE/dx distribution with a convoluted noise term.

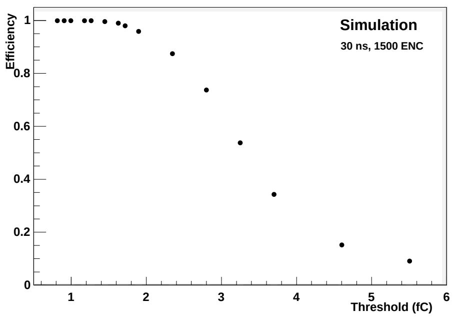


Figure 5: *Simulated S-curve*

In addition, efficiency loss due to timing effects is taken into account. A random trigger phase is generated in the interval [0,25] ns. The discriminator walk time is calculated on the basis of the input charge, the threshold and a third order CRRC shaper response curve (see figure 7 in the timing section). The sum of the trigger phase and the walk time determines the time the signal crosses threshold and thus which time bin is efficient. Simulated data were analyzed along the same lines as the data, i.e. considering only the central time bin and rejecting all events outside a narrow trigger phase window. The results in this note correspond to 300.000 events, generated assuming a peaking time of 30 ns and 1500 ENC noise.

The simulation assumes an ideal, δ function input pulse in the shaper response calculation. Therefore, it is unable to reproduce the effects of the detector bias voltage on the efficiency. The assumption is a reasonable approximation for the 240 V data, but clearly does not hold for the 80 V case, where the input signal length is of the order of the peaking time.

3.3 Binary only analysis

The introduction of the reference module provided the basis for an alternate binary-only method of analysis which did not employ telescope track or TDC timing information, as in other analyses, in an attempt to understand residual efficiencies previously observed by removing some possible sources of sample bias or common inefficiencies. Instead, efficiencies were determined from the SCT modules, including the reference module and the modules under test.

Each module under test was considered in turn, using the reference and the other two SCT modules to provide reference tracks.

[5]Ballistic deficit is defined as " the loss of output signal amplitude due to charge collection times in the detector being larger than the shaper rise time of the electronics" [14]

An 'event' was defined to be any one track event in which a hit was found in each of these three other modules, and in which a straight line could be fit to these three points within a certain confidence.

The fitted track was then projected through the module under study; if a hit was found within +/-3 strips of the predicted point the module was considered to be efficient for that event. No TDC cuts were applied. Events with tracks close to known bad channels were discarded from the sample.

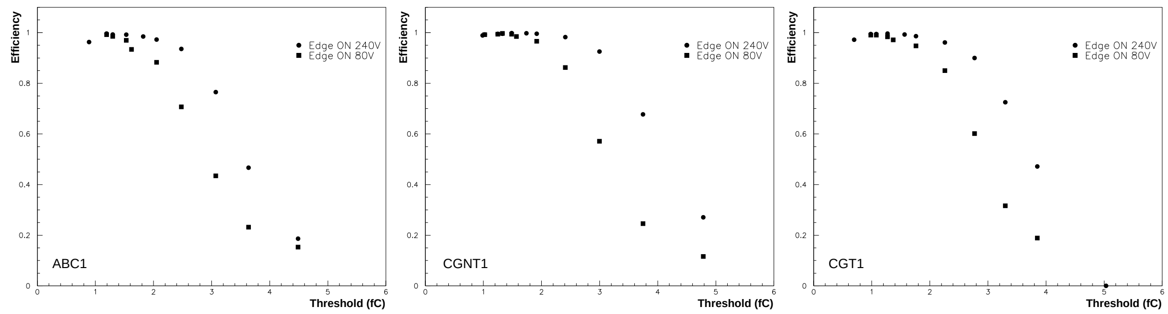


Figure 6: *Efficiency versus threshold, as obtained by a binary only analysis*

The results in figure 6 form an independent confirmation of the ballistic deficit reported by the conventional analyses. Note that, unlike other analyses, hits from all three time bins are included.

As well as providing a simple confirmation of traditional analyses, this study also indicates the feasibility of utilizing beams of intensity too high for the existing telescope planes (with microsecond shaping times), provided a number of SCT reference modules are available. Intense beams will now commonly be available at H8.

4 Timing study

This section compiles some of the recent data available on timing characteristics of the Front End electronics, both from the test beam and laboratory measurements.

In all three front end chips evaluated here the analog part consists of three functional stages: amplification, shaping and discrimination. Figure 7 shows the theoretical response of a third order CRRC shaper to two ideal (δ function) input charges. It illustrates a quite general feature of discriminator circuits: a higher charge needs less time to reach the threshold, i.e. it is discriminated faster (time walk).

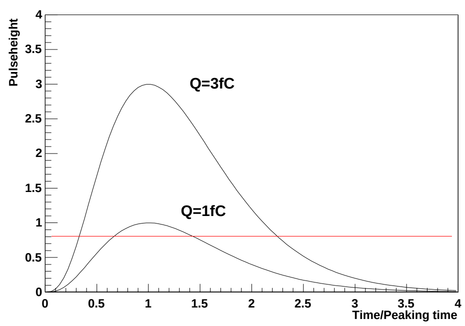
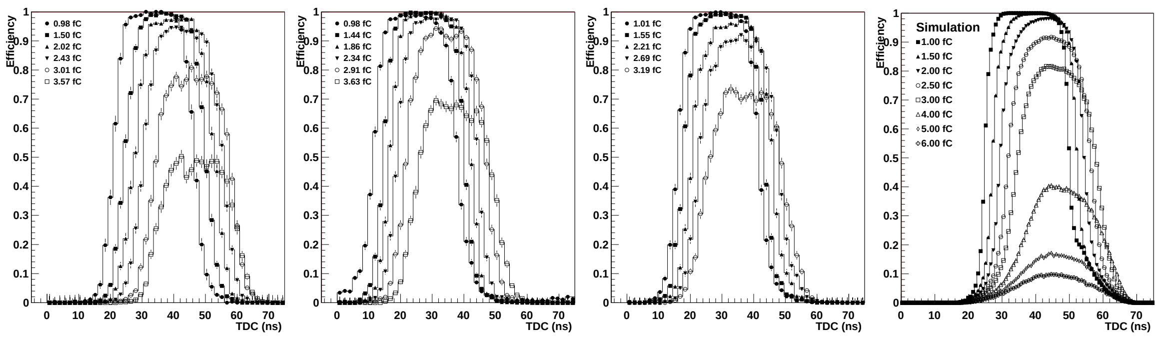


Figure 7: $CRRC^3$ *pulse shape*

The shaper should provide a fast rising pulse to maximize efficiency and a fast fall-off to provide good double pulse resolution. ATLAS specifications, see for example [1, 3], require the time walk for a fixed threshold of 1 fC and input charge between 1.25 and 10 fC to be less than 16 ns. Further, the total pulse should not exceed two clock cycles (50 ns). On the other hand, short peaking times might lead to an increase in noise and make the system vulnerable to charge loss for long input pulses (ballistic deficit). Design peaking times for the three chips are around 25-30 ns, of the order of the expected charge collection time for low voltage operation ($\sim$ 27 ns for 80 V detector bias according to equation 1).

4.1 Test beam

The timing of the test beam is governed by the random SPS beam and the 40 MHz system clock. The TDC measures the delay between charge deposition (trigger) and the sampling of the signal (determined by the clock). The previous and next time bins provide additional time windows, displaced by one clock cycle. The hit information from three time bins and the TDC value can thus be combined to reconstruct the efficiency dependence on the delay between charge deposition and sampling during three clock cycles. Figure 8 shows efficiency versus trigger phase for the three modules and various thresholds from the 240 V Edge ON scan. The central time bin corresponds to the interval from 25 to 50 ns.

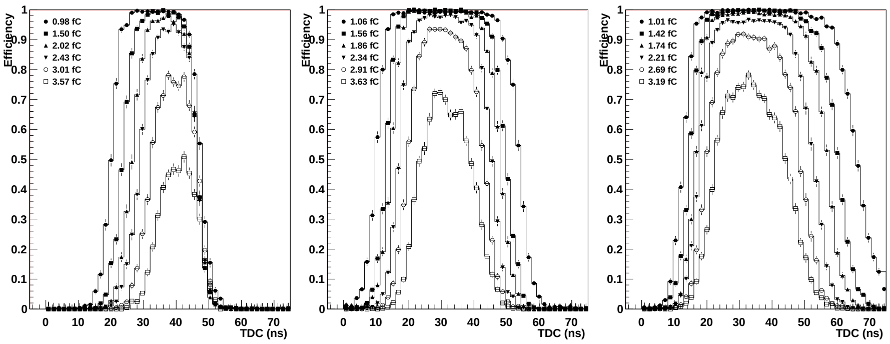


(a) (b) (c) (d)

Figure 8: *Efficiency versus trigger phase, Edge ON/240 V data: a) ABC1, b) CGNT1, c) CGT1, d) simulation*

In all three modules a clear dependence on threshold can be observed: for higher thresholds discrimination is slower, resulting in a shift of the efficiency distribution towards higher TDC values. Further, the width of the distribution is 25 ns, practically independent of threshold, as the shaper pulse is effectively cut off after one clock cycle by the edge sensing circuit. The timing dependence in figure 8 a through c can be at least qualitatively reproduced by a Monte Carlo simulation, as shown in figure 8 d. The model was briefly discussed in section 3.1.

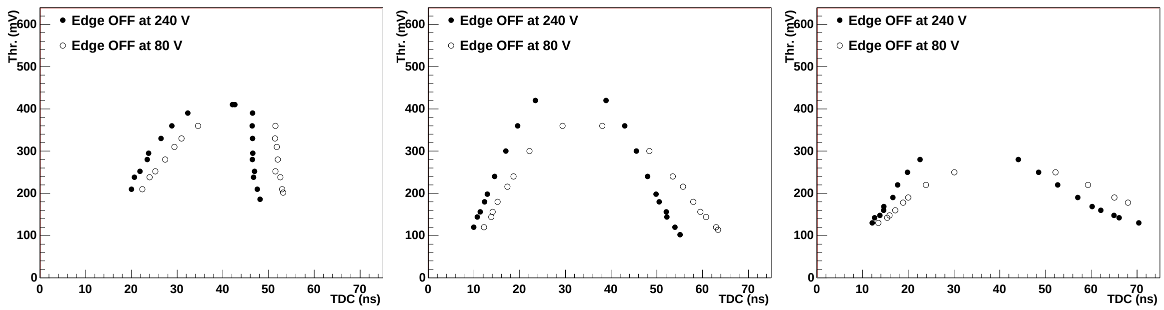
Data taken with the edge sensing circuit switched off retain more of the shaper pulse information. Figure 9 shows efficiency versus TDC for all three modules and various thresholds from the 240 V Edge OFF scan. The rising edges of these distributions are very similar to those of the Edge ON data in figure 8, but now the efficiency does not fall off until the shaper pulse drops below the discriminator threshold.



(a) (b) (c)

Figure 9: *Efficiency versus trigger phase, Edge OFF/240 V data: a) ABC1, b) CGNT1, c) CGT1*

From the edge OFF data one can estimate the discriminator input pulse shape for a typical hit by plotting the TDC value corresponding to the points of 50% efficiency versus the discriminator threshold. Figure 10 shows the pulse shapes reconstruction for both detector bias voltages.



(a) (b) (c)

Figure 10: *Reconstruction of the discriminator input pulse, edge OFF, 80 V data (filled circles) and 240 V data (closed circles): a) ABC1, b) CGNT1, c) CGT1*

The reconstructed pulse shape can be seen to differ significantly between modules. The CAFE/P shaper produces an asymmetric pulse, with a very sharp fall off. Both ABCD modules show the semi-Gaussian pulse shape of a $CRRC^3$ shaper.

Despite the differences in pulse shape, in all three modules one observes that the shaper pulse peaks at a later time and reaches a lower maximum value for 80 V data as compared to 240 V. Both effects can be explained as a ballistic deficit of the shaper. For a $CRRC^3$ shaper, reference [14] calculates the effective peaking time for flat input pulses of finite length to be:

$$t_m = \frac{T}{1 - e^{-T/\tau}} \tag{2}$$

and for the amplitude loss or relative ballistic deficit:

$$RBD \approx \frac{1}{8}(\frac{T}{\tau})^2 \tag{3}$$

where T is the input pulse length and τ the ideal peaking time (for δ function input pulses). Assuming the input pulse length to be equal to the charge collection time of equation 1, one obtains a $1/V^2$ dependence of the relative ballistic deficit on bias voltage:

$$RBD \approx \frac{1}{8}(\frac{d^2}{\mu\tau V_{bias}})^2 \tag{4}$$

where the mobility μ, ideal peaking time τ and Silicon thickness d are constant for a given module. Filling in an ideal peaking time of 25 ns, equation 4 predicts a small effect on the 240 V data: an effective peaking time of 30 ns and an amplitude loss of 1.6%. For 80 V, however, a considerable ballistic deficit is expected: the peak is shifted to 41 ns and the amplitude decreases by 15%. Considering that the $CRRC^3$ case is only a first order approximation, the simple model reproduces fairly well the observed effects. Thus, the result in figure 10 confirms the explanation of the efficiency loss of figures 3, 4 and 6 as a ballistic deficit.

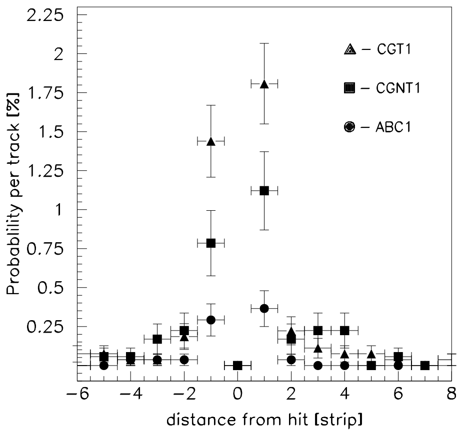


Figure 11: *Probability of after hits versus distance from track in strips*

For pattern recognition in the ATLAS system it is essential to minimize the "noise" hits, caused by the tail of a signal in the previous time bin. As seen in figure 8, the edge sensing circuit provides an effective means to limit the pulse length to one clock cycle. Still, crosstalk between strips (due to the inter strip capacitance) may induce small correlated signals in the neighboring strips. Being small, these signals can easily time walk into the next time bin. Figure 11 shows a clear increase of the probability of hits in the nearest neighbors, as compared to more distant strips. The fact that these after hits are more probable in both ABCD modules than in ABC1 agrees with the shaper pulses reconstructed in figure 10. However, even in the worst case after hits represent an increase of less than 4% per track in each layer. This will not be significant for the overall occupancy, likely dominated by noise.

4.2 Laboratory measurements

The CAFE/P and ABCD chips both have the possibility to internally generate a fast[6] calibration pulse of a range of charges with a settable strobe delay of 0-50 ns. This chapter provides some recent laboratory measurements for comparison to the shaper pulses reconstructed in the test beam.

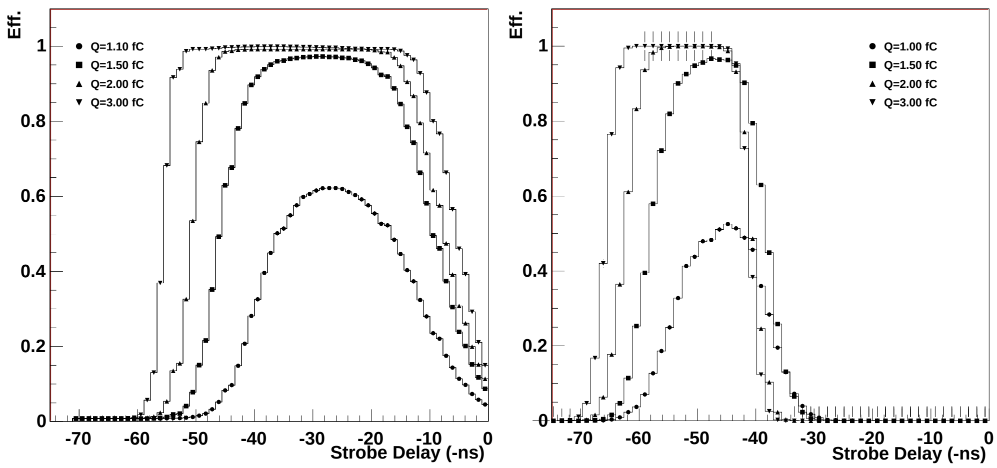


Figure 12: *Efficiency versus calibration pulse delay for chip S3 of the RLT1 module (left) and chip S2 of the ABC1 module (right)*

Figure 12 contains strobe delay scans for a fixed threshold of 1 fC and a number of input charges for one chip of the ABC1 and RLT1 modules. RLT1 is a double sided module with 12 ABCD2T chips, that should have the same characteristics as CGT1.

In order to compare these measurements to the test beam results, one should note that in the test beam the threshold was varied while the input charge was determined by the Landau charge distribution, whereas in the laboratory the input charge is varied at a fixed threshold. In addition, negative strobe delay is plotted on the X axis in order to obtain the same orientation as in the test beam TDC plots. Knowing this, the behavior is as one might expect: lower charge leads to slower discrimination, with most of the time walk concentrated in the first fC above threshold. In figure 12 one notes the fast fall off of the shaper pulse for ABC1, while the pulse shape of the ABCD2T chip is similar to the third order CRRC shape of figure 7. These results agree quite well with the pulse shapes obtained from the test beam data in figure 10. It should be noted that both methods reconstruct the signal from efficiency, which makes them insensitive to a possible undershoot of the shaper pulse.

[6] The rise time of the CAFE/P calibration pulse is less than 10 ns, according to [1]

5 Conclusions

Three independent analyses of the test beam data agree that all modules under test provide high efficiency and low noise at or near the nominal ATLAS threshold of 1 fC. After rejection of the contribution from bad channels the noise has a nearly Gaussian shape.

The residual inefficiencies are effectively removed by the introduction of a reference module at fixed bias and threshold.

A binary only analysis is certainly feasible and can provide a valuable cross check to the conventional analysis.

The table below summarizes the efficiency and noise results evaluated at thresholds near 1.0 fC. The first block of results corresponds to an analysis with only minimal bad channel rejection (2, 2 and 0 channels for ABC1, CGNT1 and CGT1 respectively). The errors quoted are statistical errors. The second block shows results after rejection of all deviating channels. For these results, the errors of have been estimated from the stability of the reference module and thus includes some, but not all, of the systematics. Results in the third block are for the binary only analysis.

Table 1: Summary of efficiency and noise results

	data	*ABC1*	*CGNT1*	*CGT1*
efficiency (%)[a]	edge ON 240 V	99.5 ± 0.1	99.6 ± 0.1	99.1 ± 0.2
occupancy	edge ON 240 V	4.7×10^{-4}	4.3×10^{-4}	2.6×10^{-4}
efficiency (%)	edge ON 80 V	98.5 ± 0.2	99.6 ± 0.2	99.3 ± 0.2
occupancy	edge ON 80 V	5.9×10^{-4}	4.8×10^{-4}	3.1×10^{-4}
efficiency (%)	240 V	99.6 ± 0.4	99.8[b] ± 0.4	99.6 ± 0.4
efficiency (%)	80 V	98.6 ± 0.4	99.5[b] ± 0.4	97.3 ± 0.4
occupancy	all data	10^{-4}	10^{-4}[b]	2×10^{-4}
Noise fit (ENC)	all data	~ 1560	~ 1470	~ 1250
efficiency (%)	edge ON 240 V	99.2[c]	99.3	99.4
efficiency (%)	edge ON 80 V	99.6[c]	99.2	99.0

[a] Results of the entire first block evaluated at optimum points. ABC1: 1.35 fC (1.24 for 80 V), CGNT1: 1.30 fC, CGT1: 1.08 fC.

[b] Efficiency and noise of CGNT1 evaluated at 1.3 fC.

[c] Efficiency of ABC1 evaluated at 1.2 fC.

At thresholds around 3 fC a considerable loss of efficiency is found for 80 V detector bias when compared to data taken at 240 V, most likely caused by a ballistic deficit of the shaper.

It is possible to reconstruct the shaper pulse from the test beam data, using the TDC information and hits from three time bins. The reconstructed pulse shapes provide further evidence for a ballistic deficit of the shaper.

References

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