TileCal Read Out Driver

ROD functionality
Front-End Mapping
Baseline Architecture
Monitor And Control Issues
Prototypes
Time Schedule

M. Nessi (CERN), J. Roldan (IFIC[1]), J.B. Romance (IFIC[1])

[1] Centro Mixto Universidad de Valencia y CSIC

ROD Functionality

GENERAL

- **Raw Data gathering** from first level de-randomizers **at the L1A event rate**
- **Standard ATLAS data format** Standard TTC signals will be present at each module providing ROD L1ID, ROD_BCID and trigger type.
- The ROD must **check** that the owner **BCID and L1ID** numbers match with the ones received from the FE. If a mismatch is detected, a flag must be set with some error code.
- Event data must be sent to ROB through the **standard ATLAS readout links** at the L1A event rate.
- **Provide a ROD busy signal** in order to **stop L1A generation**. A global OR of the busy ROD's per sub-detector has to be provided to the CTP.
- **Local Monitoring** of the data during a run without introducing dead-time or additional latency in the normal data flow.

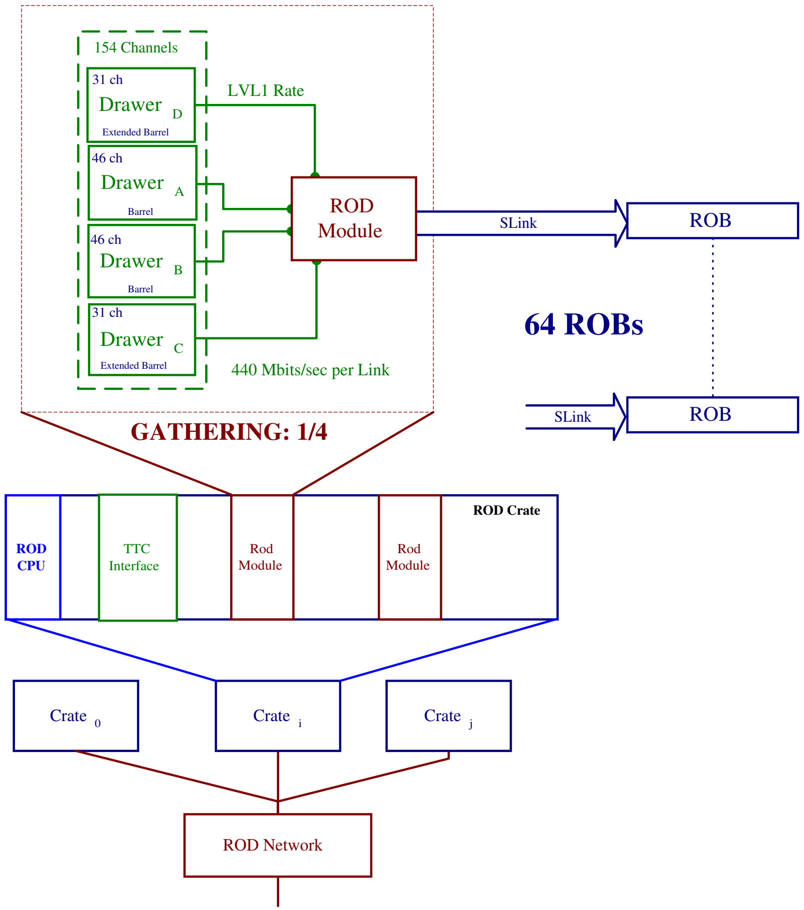
TILECAL

Beside these, Tile-Cal RODs will have the following functionality with respect to data processing:

- *Provide energy, timing and pile up estimation to the next level by optimal sample filtering*
- *Possibly to pass raw data without processing when advisable* *(pile-up, high energy events, calibration)*

Front End-ROD Mapping

- TileCal is instrumented by **DRAWERS** containing the Front-end electronics (Shaper, Level1 Adders, Bigain system, Digitizers) and the Calibration system (Integrator, Charge Injection). Each Drawer is defined and designed as a **READOUT ITEM**



- Baseline Readout maps **FOUR drawers into one ROD module** such a complete TileCal sector could be linked to a single ROD $\Delta\varphi=0.4$.

- Is desirable a **minimal data segmentation** in order to perform local data calculations over a region of interest

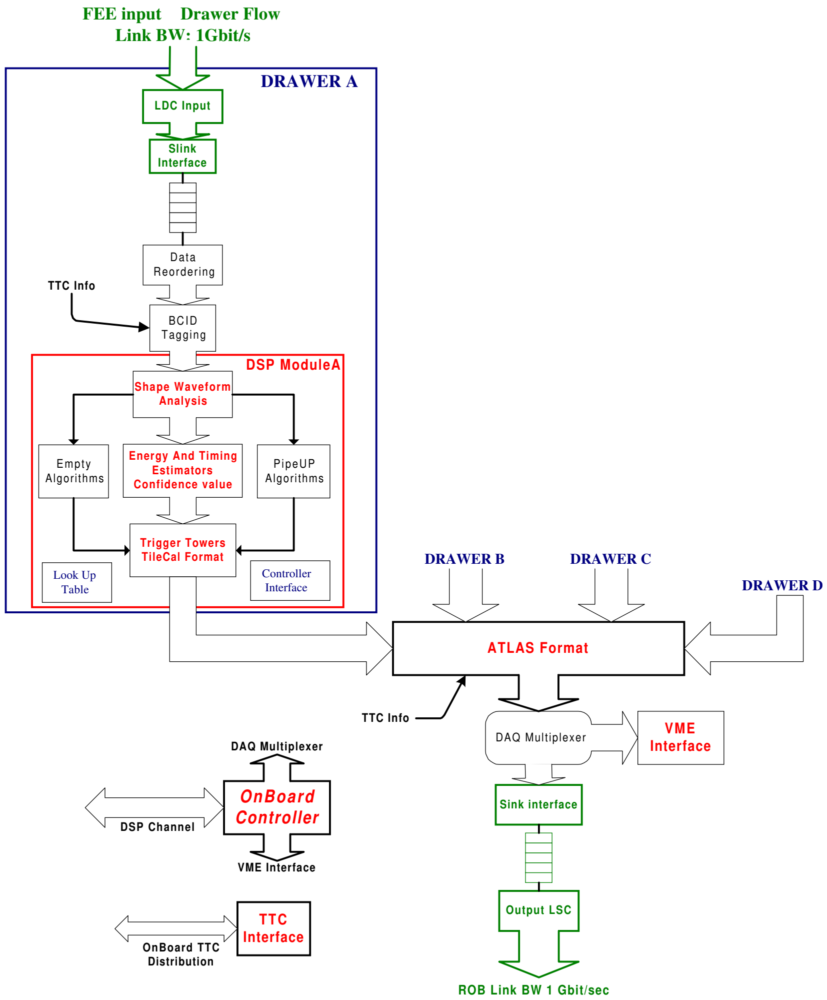
- Complete TileCal ReadOut is **256 Drawers.** ROD-ROB mapping is planned 1:1 therefore **64 RODs and ROBs** are needed.

- Following a L1A rate of 100KHz **expected Bandwidths** per Link are **440Mbit/sec (Barrel)** and **275 Mbit/sec (Extended)**. In Both cases the Header-Data fraction is 30/70 %

- **To allow an optimal readout link choice,** a S-Link baseline has been used at Front End to ROD Level for Module 0.

Juan Bautista Romance. IFIC
Thursday 19/11/98

BASELINE ROD Architecture



- Data coming from digitizers is processed by the Slink protocol and buffered in a FIFO memory in a first step. The data reordering module will extract the BCID number as well as individual samples
- The Shape Waveform Analysis will guide the processing of the buffered data, to the PileUp, Empty or Energy and timing Algorithms
- Energy and Timing values are calculated using a linear combination of the input samples. The Optimal filtering coefficients are OFF-Line calculated using information from canonical function of the signal shape and from current noise
- In a noisy environment (PileUp and Minimum bias) as LHC it is necesary to provide to ROB a confidence factor for E and T values
- Due to the different kind of data present in a single event a data preformat is done before ATLAS format
- DAQ multiplexer will be driven by On-Board controller, routing data to the VME interface or directly to the output ROB port.
- On-Board Controller will drive & monitor ROD busy and will manage I/O control functions from/to outside world

Juan Bautista Romance. IFIC
Thursday 19/11/98

Monitor And Control Issues

MONITORING

- CPU ROD Crate Controller will drive the Monitoring Data Flow
- ROD module and CPU ROD controller will fully use VME to exchange control and monitoring flow
- SPY some percentage 1-5 % of the ATLAS DAQ Data Flow
- If ROB link is disabled, the complete Data Flow will be gathered using VME ROD port at a reasonable rate, i.e. 1Khz
- SPY 100% of special triggers (calibration, ….)
- Local ROD BUSY event will be signalled using a VME interrupt
- Minimum Bias And Pile-Up Noise must be reported to provide feedback to Optimal Filtering
- Statistics related with ROD activity (CELL histogramming, Busy signal, …)

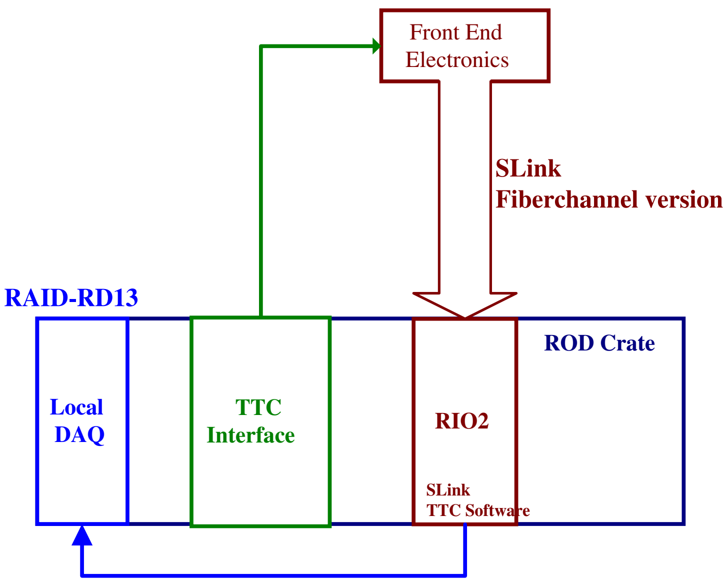
CONTROL

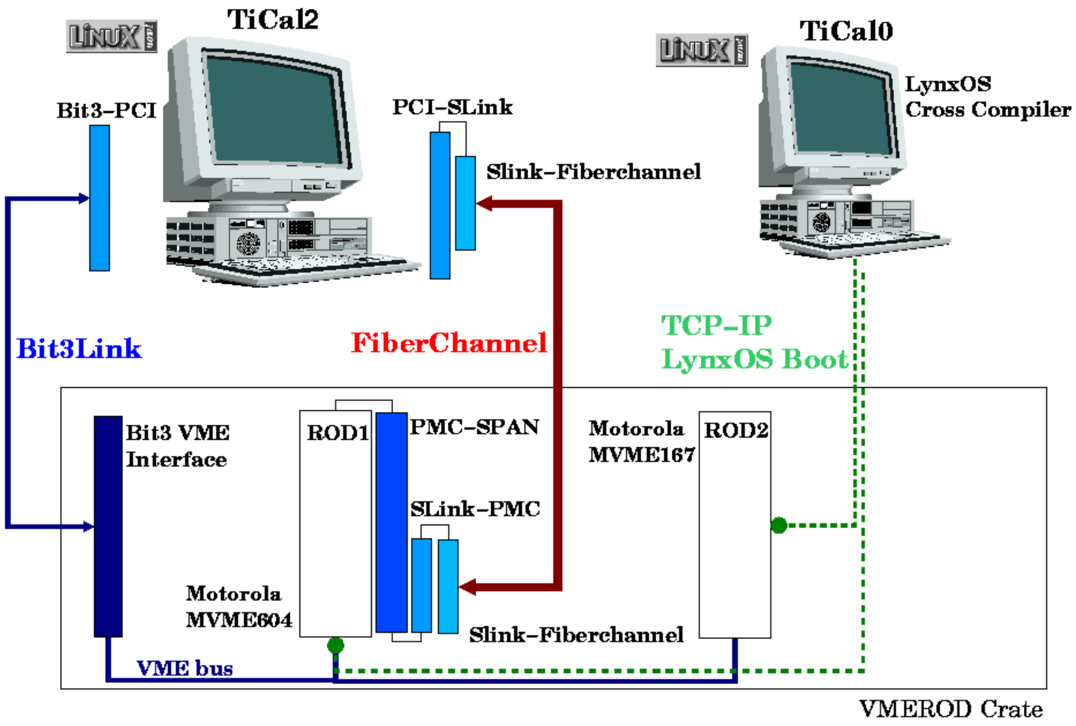
- Shared function between CPU ROD Crate Controller and each ROD board
- Software downloading from a Atlas General DataBase (DSP code, Calibration coefficients, Optimal filter parameters, etc …)
- On Physics or Calibration triggers different programs will be VME transferred on-line to DPSs
- A Protocol between ROD Crate Controller and the whole Calibration System must be defined
- Is desirable an extra TRIGGER DAQ Management
  - Test and check system functionality
  - Perform Calibration RUNs
- Each ROD crate will be accessed by a “ROD NETWORK”

Juan Bautista Romance. IFIC

ROD Prototypes

- Current MiniROD prototypes allow evaluation of different technologies of Main ROD Module items such Drawer Core Processing (Software and Hardware) and the Front-End and ROB Readout Links
- Can be tested at Test-Beam or Stand-alone environments . And seems well fitted to ATLAS DAQ-1
- Are based in commercial 6U VME boards using a PowerPC as host controller where multiple PMCs sites are available, customised or commercial mezzanines can be fully tested
- Two systems are already available at Test-Beam (CERN), based in a RIO2 board, and at Valencia (ROD Lab), based in a MVME2604+PMCSpan system





Juan Bautista Romance. IFIC
Thursday 19/11/98

- A first General TileCal ROD requirements work document is already available
- Feedback from TileCal collaboration is being used to develop a complete document defining the functions and requirements of the basic items of the ROD system.
- Main **open questions** are related with the **algorithms to estimate energy and timing**. ROD is considered as a data compressor when front-end data could be lost. A detailed work should be done using Module-0 experience and Montercalo simulation.

TIME SCHEDULE

➢ Mini ROD Test-Beam Calibration	1998-2002
➢ ROD module- 0	1998-2000
➢ Final Design, Design Review	end of 2000
➢ Production, Assembly and Procurement	2001-2002
➢ ROD Commissioning	2003

Juan Bautista Romance. IFIC
Thursday 19/11/98