TileCal ROD Crate Controller VME Master Mapping Configuration

How To

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Abstract

This is the proposal of a PCI to VME Master Mapping Window configuration of the CT VP-110 single board computer to access the ROD crate modules in the Tile Calorimeter Read Out Driver of the ATLAS detector.

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1 Introduction

This document describes the VME mapping of the ATLAS Single Board Computer VP-110/01x and how to configure the memory mapping of the VME windows to PCI address space.

The configuration of the SBC is very important since it will be the final ROD controller for the ATLAS-Tilecal[1] ROD crate, and will be the responsible for the control and configuration of the whole ROD crate modules (ROD, TBM, etc …[2])

In the reference chapter, it's also detailed all the information needed to install, configure, and network boot this device [5][6][7][8][9][10][11].

2 VME Master Mapping on CT VP-110 for Tilecal ROD

The CT-VP 110 has a PCI to VME bridge controller (Tundra UNIVERSE II chip) to access from PCI memory to VME memory space. The proposed configuration of the mapping windows for the Tilecal ROD Controller[1] is shown in Table 2. You can see the present configuration of your SBC in linux system file ***/proc/iomem***.

The global mapping of the ROD crate modules based on the base address built from geographical address pins is shown in Table 1

Crate Slot Number	Geographical address pin[2] (A28..A24)						VMEBus Adress (32 bit hex)
	GAP#	GA4#	GA3#	GA2#	GA1#	GA0#	
1	1	1	1	1	1	0	01000000
2	1	1	1	1	0	1	02000000
3	0	1	1	1	0	0	03000000
4	1	1	1	0	1	1	04000000
5	0	1	1	0	1	0	05000000
6	0	1	1	0	0	1	06000000
7	1	1	1	0	0	0	07000000
8	1	1	0	1	1	1	08000000
9	0	1	0	1	1	0	09000000
10	0	1	0	1	0	1	0A000000
11	1	1	0	1	0	0	0B000000
12	0	1	0	0	1	1	0C000000
13	1	1	0	0	1	0	0D000000
14	1	1	0	0	0	1	0E000000
15	0	1	0	0	0	0	0F000000
16	1	0	1	1	1	1	10000000
17	0	0	1	1	1	0	11000000
18	0	0	1	1	0	1	12000000
19	1	0	1	1	0	0	13000000
20	0	0	1	0	1	1	14000000
21	1	0	1	0	1	0	15000000

Table 1: Base Address for ROD Crate modules based in geographical addressing

[1] CT VP-110 933MHz, 512 Mbyte RAM

[2] GA0# - GA4# : Low level active binary code that indicates the slot number
GAP# parity

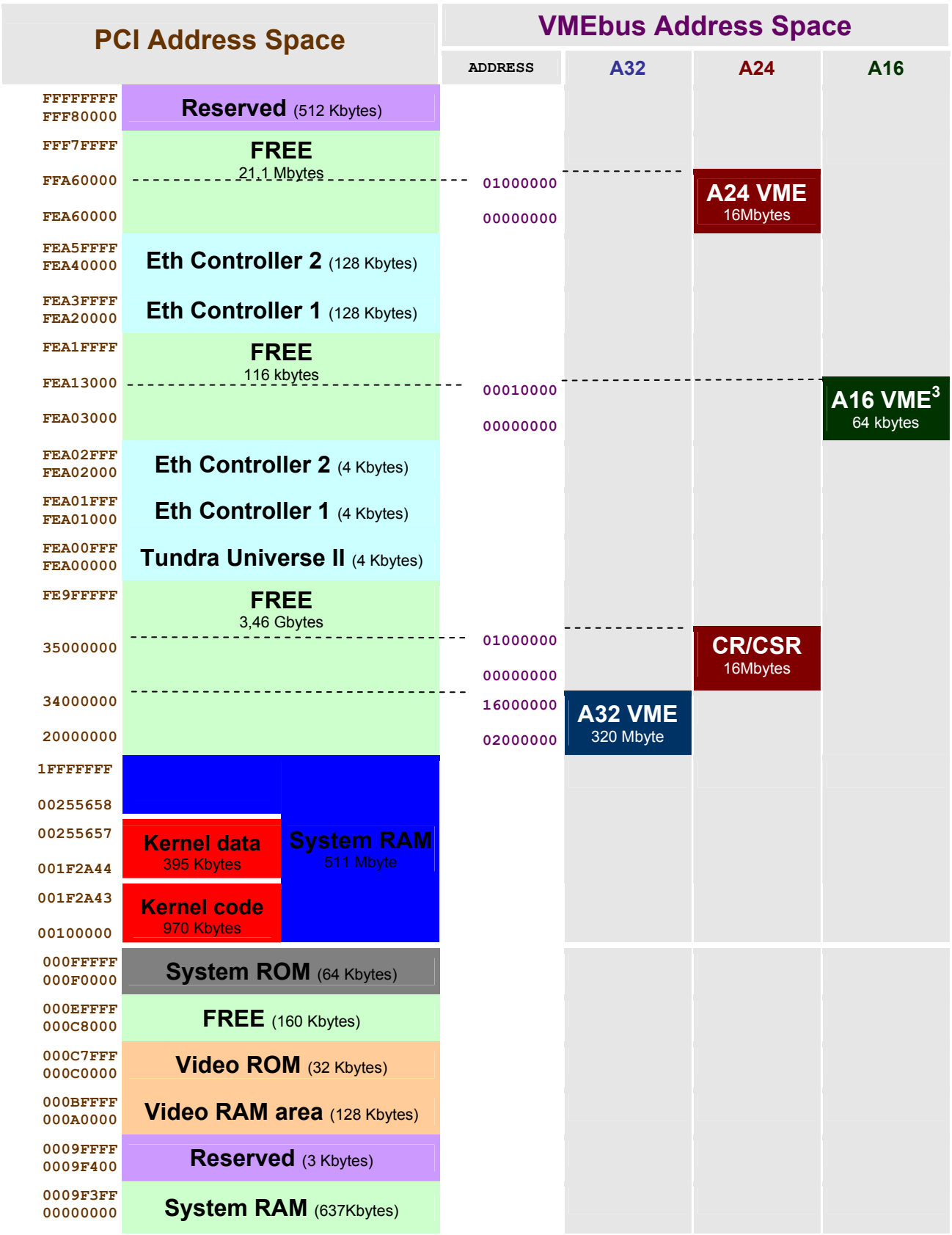

Table 2: Proposed PCI to VME memory windows for CT VP110 512 Mbytes RAM

[3] This configuration is also valid for the Tilecal TTC crates [2]. Really, for TTC crate controller is only needed 16 Mbytes of A24 (D32) space and 64 Kbytes A16 space for special modules.

The window needed for 20 slots (slot 2 to 21[4]) is: 2^{24} x 20 = 320 Mbytes

To set-up this configuration we must use the application ***vmeconfig***[4] included in the package ***vme_rcc***[4][10] of the ATLAS-Dataflow[3] repository.

The command to type is: ***vmeconfig –i my_vmetab***

Where:

-i means interactive configuration

my_vmetab is the file to store the configuration

When you have your ***vmetab*** file configured you must execute at boot time: ***vmeconfig –a my_vmetab,*** where ***–a*** means automatic load of configuration file.

The configuration proposed in Table 2 and applied with ***vmeconfig*** utility is summarized in the following Table 3:

Master Map Decoder Number	VME Address range	PCI Address range	Enabled	WP	VME Address space	VME Data Width	AM	PCI space
0	**00000000-00010000**	**FEA03000-FEA13000**	**Yes**	No	**A16**	**D32**	User/Data	MEM
1	**00000000-01000000**	**FEA60000- FFA60000**	**Yes**	No	**A24**	**D32**	User/Data	MEM
2	**02000000-16000000**	**20000000-34000000**	**Yes**	No	**A32**	**D32**	User/Data	MEM
3	**00000000-01000000**	**34000000-35000000**	**Yes**	No	**CR/CSR**	**D32**	User/Data	MEM
4	00000000-00000000	00000000- 00000000	No	No	A32	D32	User/Data	MEM
5	00000000-00000000	00000000- 00000000	No	No	A32	D32	User/Data	MEM
6	00000000-00000000	00000000- 00000000	No	No	A32	D32	User/Data	MEM
7	00000000-00000000	00000000- 00000000	No	No	A32	D32	User/Data	MEM

Table 3: Universe chip master map decoders configuration for ROD Crate controller

The VP-110 also allows dynamic VME mapping configuration. This is useful if any application needs more memory than the one we could configure statically with the limited number of map registers. Nevertheless, here is proposed the static configuration at boot time since we can address all the ROD crate VME modules, and saving thus the latency introduced with dynamic chipset configuration.

[4] Slot 1 will be used by crate controller CT VP-110

3 Acronyms

RCC : ROD Crate Controller

PCI : Peripheral Component Interconnect

RAM : Random Access Memory

ROD : Read Out Driver

ROM : Read Only memory

SBC : Single Board Computer

VMEbus : Versa Modular Eurocard bus

4 References

[1] **Tile Calorimeter TDR**, ATLAS/Tile Calorimeter collaboration, CERN-LHCC9642.

[2] **Hardware and Software Requirements**, J. Castelo et al., ATL-TILECAL-2005-002.

[3] **ATLAS Dataflow repository,**
http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/ROS/code_repository/

[4] **Implementation and release notes for the VMEbus API on Linux based processors from Concurrent technologies**, M. Joos and J. Petersen.,
https://edms.cern.ch/file/325729/4/vme_cct_linux.pdf

[5] **VP 110/01x Specification Sheet**, Concurrent Technologies,
http://www.gocct.com/sheets/vp11001x.htm

[6] **VP110 user's guide**,
http://atlas.web.cern.ch/Atlas/private/DIG/RCC/vp110_manual.pdf

[7] **VP-110 Network based booting**,
http://atlas.web.cern.ch/Atlas/private/DIG/RCC/netboot.pdf

[8] **VP110 installation**, http://atlas.web.cern.ch/Atlas/private/DIG/RCC/install.htm

[9] **VP-110 RS232 trouble shooting**,
http://atlas.web.cern.ch/Atlas/private/DIG/RCC/falco.htm

[10] **VMEbus and the vme_rcc S/W package for the VP110**,
http://cdsweb.cern.ch/search.py?recid=710506

[11] **VMEbus Single Board Computers for use as ROD Crate Controllers**,
http://atlas.web.cern.ch/Atlas/private/DIG/RCC/