MOTHER BOARD REGISTERS
GEOGRAPHICAL ADDRESS + A(10:7) + INTERNAL ADDRESS(5 bits)

DEC	INTERNAL BIN	INTERNAL Hex	R/W	FONCTION	BITS	VMEDATA	init value			
		LOCAL Register (A10:7) = 0000								
0	0	0	W/R	base address register	31:0					
1	1	4	W	reset general		sent to all chips				
2	10	8	R	status	9	data_bus externe au chip vme				
					8	quick answer				
					4	busy vme bloque busy initialisation				
					3:0	pu-ready				
3	11	C	R	board identificator	7:0	switch hard on board				
4	100	10	W	force busy	0	**1 b**usy forced to 1 (default during initialisation)				
					1	**1** data bus extern chip VME(vmeconfig)				
					2	**1** quick answer 2clock(vmeconfig)				
					3	**1** quick answer 4clock(vmeconfig)				
				Jtag						
15	1111	3C		version						
		BUSY Registers (A10:7) = 0000								
1	10001	44	W	reset and control					0	pu1_busy1
									1	pu2_busy1
									2	pu3_busy1
					16	send sreq			3	pu4_busy1
					8	write duration busy to fifo	1xx		4	pu1_busy2
					4	reset timing	1x		5	pu2_busy2
					3	reset interval wr fifo counter	8		6	pu3_busy2
					2	reset sreq counter	4		7	pu4_busy2
					1	reset busy duration	2			
					0	reset fifo	1			
2	10010	48	R	status	25	busy_active (idem..)	2xxxxxx			
					24	busy_pu (idem …)	1xxxxxx			
					23:16	mask busy(idem..)	FFxxxx			
					14:13	fifo FF 4xxx EF 2xxx				
					12	enable sreq(idem..)	1xxx			
					11	sreq out	8xx			
					10	sreq in	4xx			
					9	enable busy(idem ..)	2xx			
					8	busy out	1xx			
					7:0	busy in	FF			
3	10011	4C	W/R	miscellaneous	23:16	mask busy	FFxxxx		16	pu1_busy1
					12	enable SREQ	1xx		17	pu2_busy1
					9	enable busy	2x		18	pu3_busy1
					1	1 mode normal		0	19	pu4_busy1
					1	0 mode manual (read fifo by VME authorized)			20	pu1_busy2
					0	busy source: 1 = PU, 0 = VME		0	21	pu2_busy2
4	10100	50	W/R	interval wr fifo	31:0	write to fifo each (div_clock * value)		1	22	pu3_busy2
5	10101	54	W/R	sreq max	31:0	sreq sent if count_busy > value		1	23	pu4_busy2
6	10110	58	W/R	div clock	7:0	busy count each (100 nS + 25nS*(n -1))		1		
7	11000	60	R	read fifo	19:18	full fifo 8xxxx / empty fifo4xxxx before reading fifo				
					17:16	full fifo 2xxxx/ empty fifo1xxxx after reading fifo				
					15:0					
8	10111	5C	R	read duration busy	15:0					
9	11001	64	R	read sreq counter	31:0					
A	11010	68	W	send busy	15:8	send busy	FFxx			
		IRQ Registers (A10:7) = 00011								
1	00001	184	W	reset	13:0	reset pending and request IRQ by VME				
2	00010	188	R	status1	13:0	state of input IRQ (cf list) before mask	FEXX XXXX			
					23:17	state of **REAL** output IRQ after enable	FE XXXX			
2	00011	18C	R	status2	13:0	state of interrupt request not sent	FEXX XXXX			
					28:17	state of interrupt request to be sent	FE XXXX			
3	00100	190	W/R	mask/enable	16	enable irqout	FE XXXX			
					13:0	mask irqinput	3FFF			
9	00101	194	W/R	mapping 1 ouput IRQ	7:1	1 output IRQ				
					10:8	1 output coded				
						102=IRQ1,204=IRQ2, 308=IRQ3, 410=IRQ4				
						520=IRQ5, 640=IRQ6				
10	10000	1C0		INPUT IRQ STATUS ID	7:0	pu1_irq1(0) defaut 1			0	pu1_irq1
	10004	1C4				pu1_irq2(1) defaut 2			1	pu1_irq2
	10010	1C8				pu2_irq1(2) defaut 3			2	pu2_irq1
	10011	1CC				pu2_irq2(3) defaut 4			3	pu2_irq2
	10100	1D0				pu3_irq1(4) defaut 5			4	pu3_irq1
	10101	1D4				pu3_irq2(5) defaut 6			5	pu3_irq2
	10110	1D8				pu4_irq1(6) defaut 7			6	pu4_irq1
	10111	1DC				pu4_irq2(7) defaut 8			7	pu4_irq2
	11000	1E0				oc1_irq(8) defaut 9			8	oc1_irq
	11001	1E4				oc2_irq (9) defaut 10 A			9	oc2_irq
	11010	1E8				oc3_irq (10) defaut 11 B			10	oc3_irq
	11011	1EC				oc4_irq(11) defaut 12 C			11	oc4_irq
	11100	1F0				irq_temp(12) defaut 13 D			12	temp_irq
	11101	1F4				irq_busy(13) defaut 14 E			13	busy_irq
		BOOT PU Registers (A10:7) = 00001								
DEC	INTERNAL BIN	INTERNAL Hex	R/W	FONCTION	BITS		init value			
		TTC Registers (A10:7) = 0010								

0	0	100	R	dummy						
1	1	104	W/R	ctrl	7:5	pulses 7=TTC_reset, 6=clear status, 5=flush				
					4	L1A mode double pulse				
					3	clk-sel 0: local, 1 ttcrx				
					2:0	0= VME mode,1 local mode, 2 TTC mode				
2	10	108	W	BCID register	12:0					
3	11	10C	W	EVID register	32:0					
4	100	110	W	ttype register	8:0					
5	101	114	R	Status register	25:24	25 TTCclock present 24 TTRX working				
				DL_ERR	23:16	non double L1A count in double_l1a mode				
				DB_ERR	15:8	bouble error strobe count				
				SIN_ERR	7:0	single error strobe count				
PU Transparent Registers (A10:7) = 0100 -> 0111						pu-nul6				
0	0	200	W/R	dummy 32 bits register						
1	1	204	W	reset	5:4	5:fifo_int 4:fifo-ext				
					3:2	reset feb2s, feb1s				
					1:0	reset feb2, feb1				
2	10	208	R	status	5:0	paf2, paf1, full2, full1, empty2, empty1 EXT				
					11:8	full2, full1,empty2 ,empty1 INT				
					16	config(0)				
4	100	210	W/R	configuration register	31:16	pulse length	FFFFxxxx			
					0	**1**: fifo1-2< = feb1-2, **0**: fifo1-2 <= feb1-2S				
					1	**1**: led_ini: 40 MHz, 80MHz WENN fifo				
					1	**0** : errors et link ready				
5	101	214	R	read fifo_int						
6	110	218	W/R	pulse and set/reset busy	9:8	set reset9: irq2 8: irq1	3xx			
					5:4	set reset 5: busy2 4: busy1	3x			
					1:0	pulse busy 1 busy2, 0: busy1	3			
1f	11111	2FC	W/R	version						
OUTPUT CONTROLER Registers (A10:7) = 1000 -> 1011										
0	0	400	R	status						
1	1	404	W	reset		REGR				
2	10	408	W/R	config		config				
4	100	410	W	format version number reg		REGF				
8	1000	420	W	source identifier reg		REGI				
16	10000	440	W	detector event type reg		REGE				
18	10010	448	W	etector format version number reg		REGD				
STAGING Registers (A10:7) = 1100 -> 1111, 60-68-70-78										
	led_high					sans feb alumée/ avec feb (1 ou 2) count				
	led_low					sans feb emit / avec feb (1 ou 2) count				
0	0	600	W/R	dummy 32 bits register						
1	1	604	W	commande	18	rst min _max temp	4xxxx			
					17:16	rst count_feb2, feb1 error	3xxxx			
					11:8	error link2s, link1s----link not ready link2s, link1s	Fxx			
					7:6	error link2, link1	CX			
					5:4	link not ready link2, link1	3X			
					3:2	reset link2s, link1s	C			
					1:0	reset link2, link1	3			
2	10	608	R	status	31:30	feb2 cav, feb1 cav				
					29:28	feb2 dav, feb1 dav				
					27:24	feb2_lnk_rdy, feb1_lnk_rdy, feb2_error,feb1-error				
					23:20	fifo stag flag23 :full2, 22 full1,21 empty2, 20 empty1				
					17:16	busy_delay, busy_emit	3xxxx			
					15:8	count_feb2_error	FFxx			
					7:0	count_feb1_error	FF			
4	100	610	W/R	configuration register	9:0	nb mots/event	3FF			
					31:16	nb de events	FFFFxxxx			
5	101	614	W/R	config2 register	25:16	delay entre events	3Fxxxx			
					14	**1** input non stoppées si Glink non locké	4xxx			
					13	**1** infinite loop	2xxx			
					12	**1** block emision avec spare0 from PU	1xxx			
					11	**1** feb input with bit 16 to PU	8xx			
					10	**1** feb input with bit 16= read fifostag	4xx			
						1 leds =counter **0** high= light low= start_emit				
					9	**1** feb_input to data2	2xx			
					8	**1** feb_input to data1	1xx			
					6	**0** pu is ready	4x			
				stag2puOK	5	en mode staging 1 out sur own PU, 0 sur autre	2x			
				staging	4	1 mode staging 0 pas en staging	1x			
				sel_out	3	0=> datafeb2s=0, 1=>datafeb2s=data_ram(31-16)	8			
					2	0=> datafeb2=0, 1=>datafeb2=data_ram(31-16)	4			
					1	0=> datafeb1s=0, 1=>datafeb1s=data_ram(15-0)	2			
					0	0=> datafeb1=0, 1=>datafeb1=data_ram(15-0)	1			
6	111	61C	W/R	adresse de départ	9:0					
7	110	618	W/R	data dans Ram						
8	1000	620	W	start emission	0					
9	1001	624	W/R	link_condfig	5:4	div1,div0				
					3,2	feb_eqn 2,1				
					1:0	feb_flag 2,1				
16	10000-10111	740=>75C	R	temp	23:0	23:16 max, 15:8 min, 7:0 actuel				
	11111	6FC		version						