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TTC PMC receiver (TTCpr)
Preliminary Description

The TTC PMC receiver (TTCpr) is designed so that the functionality of the card may be easily altered. The PMC has an Altera 10K30A with the configuration file stored in an adjacent socketed serial PROM. Other components on the card are the TTCrx, an AMCC 5933 which manages the interface to the PCI port and four blocks of FIFO each 16 bits wide by 8K words deep. The FIFO's are written on 16 bit buses, but read during DMA as 4 byte words. The flexibility of the card derives from tying all relevant inputs and outputs of the TTCrx, 5933, and FIFO to I/O's on the 10K. Accordingly the functionality of the PMC depends only on the configuration of the 10K, which depends only on the configuration PROM.

The TTCpr in the current preliminary design reads the pci-addon mailboxes, writes the addon-pci mailboxes, and handles addon-initiated FIFO bus mastering. The mailbox read/writes occur in response to an IRQ* which is raised by the PCI write to pci-addon mailbox 4. The addon-initiated DMA occurs in response to the number of events which have been received equalling the event threshold.

Each L1A results in two 4 byte words being written to FIFO 0,1. The low 24 bits of the first word is the Event Number. The Bunch Crossing Number is written in the low 12 bits of the second word and the Trigger Type is stored in the low byte of the top half of the second 32 bit word.

The assignment of mailboxes is as follows:

addon incoming mailbox 2	bits 0-31	event threshold
addon incoming mailbox 4	bits 0-31	DMA starting address