| TBM VME Addresses | | | |
|---|---|---|---|
| **Hexadecimal VME Address Offset** | **Function** | **Write / Read** | **Bits** |
| 0 | Simple Register | W / R | 15..0 |
| 4 | Reset TBM ( 3 microseconds ) | W | - |
| C | Read TBM Serial Number | R | 5..0 |
| 3C | Read FPGA Version ( 6084 on November 10th 2004 ) | R | 15..0 |
| 184 | Reset Each of the 4 Interruptions<br>( IRQ Calib bit 0, Busy ON bit 1, Busy OFF bit 2, TTCrx = bit 3 ) | W | 3..0 |
| 188 | Read Interruptions before Mask<br>( IRQ Calib bit 0, Busy ON bit 1, Busy OFF bit 2, TTCrx = bit 3 ) | R | 3..0 |
| 18C | Read Interruptions not sent<br>( IRQ Calib bit 0, Busy ON bit 1, Busy OFF bit 2, TTCrx = bit 3 ) | R | 3..0 |
| 190 | Enable IRQ Out and<br>Mask Register<br>( IRQ Calib bit 0, Busy ON bit 1, Busy OFF bit 2, TTCrx = bit 3 ) | W / R | 15<br>3..0 |
| 194 | Code for TBM IRQ Level and<br>TBM IRQ Line<br>( 102=IRQ1,204=IRQ2, 308=IRQ3, 410=IRQ4, 520=IRQ5, 640=IRQ6 ) | W / R | 10, 9, 8<br>7..1 |
| 1C0 | Interruption Vector for IRQ Calibration | W / R | 7..0 |
| 1C4 | Interruption Vector for IRQ Busy ON | W / R | 7..0 |
| 1C8 | Interruption Vector for IRQ Busy OFF | W / R | 7..0 |
| 1CC | Interruption Vector for IRQ TTCrx | W / R | 7..0 |
| | | | |
| 240 | Control Register | W / R | 7..0 ( see details ) |
| 244 | Read Status Register | R | 13..0 ( see details ) |
| 248 | Discounter L1A | W / R | 15..0 |
| 24C | Clear Counter L1A | W | - |
| 250 | Read Counter L1A ( 16 LSB ) | R | 15..0 |
| 254 | Read Counter L1A ( 16 MSB - Overflow in Status Register ) | R | 15..0 |
| 258 | Busy Mask Register | W / R | 15..0 |
| 25C | Read Busy Signals Before Mask | R | 15..0 |
| 260 | Read Busy Signals After Mask | R | 15..0 |
| 264 | Set Busy | W | - |
| 268 | Clear Busy ( clears User Busy and Calib Busy ) | W | - |
| 26C | Set Lemo3 | W | - |
| 270 | Clear Lemo3 | W | - |
| 274 | Read CERN TBM Identifier ( 0303 ) | R | 15..0 |
| 278 | Read CERN Identifier ( 8003 ) | R | 15..0 |
| 27C | Read Crate Serial Number | R | 4..0 |
| 280 | Reset TM-Bus between TBM and Transition Modules TM | W | - |
| 284 | Select TM for reading its serial number / Read Selected TM | W / R | 4..0 |
| 288 | Read Selected TM Serial Number | R | 7..0 |
| 28C | Read CERN TM Identifier ( 0304 ) | R | 15..0 |
| 290 | Read FPGA Version ( 2311 on November 23rd 2004 ) | R | 15..0 |
| 294 | Reset TTCrx | W | - |
| 298 | Generate Interruptions ( fugitive action )<br>Bit 0 generates IRQ Calib<br>Bit 1 generates IRQ Busy ON<br>Bit 2 generates IRQ Busy OFF<br>Bit 3 generates IRQ TTCrx | W | 3..0 |

## Details

| Bit Number | Control Register |
|---|---|
| 0 | Enable IRQ Calib |
| 1 | Enable IRQ Busy ON |
| 2 | Enable IRQ Busy OFF |
| 3 | Enable IRQ TTCrx |
| 4 | Enable Busy Calib |
| 5 | Enable Counter L1A |
| 6 | - |
| 7 | Enable TM-Bus |

| Bit Number | Status Register |
|---|---|
| 0 | IRQ Calib enabled |
| 1 | IRQ Busy ON enabled |
| 2 | IRQ Busy OFF enabled |
| 3 | IRQ TTCrx enabled |
| 4 | Busy Calib enabled |
| 5 | Counter L1A enabled |
| 6 | L1A Counter Overflow |
| 7 | TM-Bus enabled |
| 8 | OR of ROD Busy Signals Before Mask |
| 9 | OR of ROD Busy Signals After Mask |
| 10 | User or Calibration Busy |
| 11 | Crate Busy (OR of 9 and 10) |
| 12 | Lemo3 |
| 13 | TTCrx Ready |