S32PCI64

32-bit S-LINK to 64-bit PCI interface

Users Guide

Authors

Wieslaw Iwanski - INP Cracow

Erik van der Bij - CERN Geneva

Date

20 February 2002

EDMS document ID

249657

Table of Contents

S32PCI64 1

PCI CONFIGURATION REGISTERS 3

OPERATION REGISTERS 9

S32PCI64

Introduction

The 32-bit S-LINK to 64-bit PCI interface (S32PCI64) can move data from a 32-bit S-LINK Link Destination Card to a 32-bit or 64-bit PCI bus that runs at 33 MHz or at 66 MHz. The interface can only be used in 3.3 Volt PCI slots; the LDC plugged on the S32PCI64 has to be of a 3.3 Volt type.

The host processor can set up the interface to receive up to fifteen S-LINK data blocks by writing to the Request FIFO the addresses where the data has to be stored and the maximum length of each data packet to be received (figure 1). After this, the interface can receive this data without needing any intervention of the processor. After reception of the data, the host processor can read from the Acknowledge FIFO the S-LINK control words and the length of the data block received.

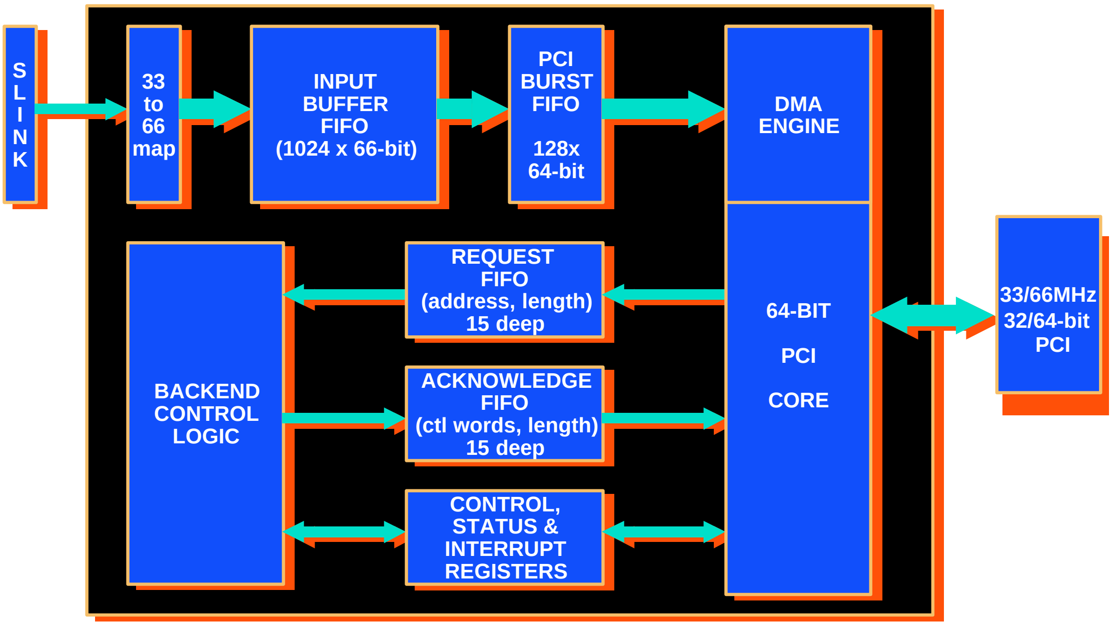
S L I N K
33 to 66 map
INPUT BUFFER FIFO (1024 x 66-bit)
PCI BURST FIFO 128x 64-bit
DMA ENGINE
REQUEST FIFO (address, length) 15 deep
ACKNOWLEDGE FIFO (ctl words, length) 15 deep
CONTROL, STATUS & INTERRUPT REGISTERS
BACKEND CONTROL LOGIC
64-BIT PCI CORE
33/66MHz 32/64-bit PCI

Figure 1: block diagram of the S32PCI64

There are versions of the interface available in which specific Link Destination Card logic is integrated on the printed circuit board. There are in total three versions:

- Generic S-LINK LDC connector
- Single ODIN LDC (128 MB/s)
- Double ODIN LDC (160 MB/s)

Features

The main features of the interface are:

- highly autonomous data reception
- reception speed independent of interrupt or polling latency
- interrupt generation selectable on reception of one or several data blocks, link down, space available in Request FIFO and others.
- control words stored independently from data
- error information stored in the control words
- programmable word and byte swapping of data words
- 32-bit S-LINK (3.3V S-LINK only)
- 32-bit and 64-bit PCI bus (3.3V PCI bus only)
- 33 and 66 MHz MHz PCI clock speed
- 32-bit PCI-bus addressing

PCI Configuration registers

The PCI configuration registers are the standard registers that every PCI compatible card has. Detailed information on the usage of those registers can be found in the PCI Specification

Vendor Identification Register (VID)

Register name	Vendor Identification (VID)
Address offset	00-01h
Boot-load	10DCh (CERN)
Attribute	Read Only (RO)
Size	16 bits

Device Identification Register (DID)

Register name	Device Identification (DID)
Address offset	02-03h
Boot-load	0012h (32-bit S-LINK to 64-bit PCI interface, S32PCI64)
Attribute	Read Only (RO)
Size	16 bits

PCI Command Register (PCICMD)

Register name	PCI Command (PCICMD)
Address offset	04-05h
Boot-load	0000h
Attribute	Read/Write (R/W on 6 bits, Read Only on all others)
Size	16 bits

PCI Status Register (PCISTS)

Register name	PCI Status (PCISTS)
Address offset	06-07h
Boot-load	0080h
Attribute	Read Only (RO), Read/Write Clear (R/WC)
Size	16 bits

Revision Identification Register (RID)

Register name	Revision Identification (RID)
Address offset	08h
Boot-load	43h (version 4.3 - 19 February 2002)
Attribute	Read Only (RO)
Size	8 bits

Class Code Register (CLCD)

Register name	Class Code (CLCD)
Address offset	09-0Bh
Boot-load	028000h (network controller/other communication device/programming interface 00h)
Attribute	Read Only (RO)
Size	24 bits

Cache Line Size Register (CALN)

Register name	Cache Line Size
Address offset	0Ch
Boot-load	00h
Attribute	Read Only (RO)
Size	8 bits

Latency Timer Register (LAT)

Register name	Latency Timer (LAT)
Address offset	0Dh
Boot-load	FFh
Attribute	Read/Write (R/W)
Size	8 bits

Header Type Register (HDR)

Register name	Header Type (HDR)
Address offset	0Eh
Boot-load	00h (Single function, Format field 0)
Attribute	Read Only (RO)
Size	8 bits

Built-in Self-test Register (BIST)

Register name	Built-in Self-test (BIST)
Address offset	0Fh
Boot-load	00h
Attribute	D7, D5-0 Read Only, D6 as PCI bus write only
Size	8 bits

Base Address Register 0 (BADR0)

Register name	Base Address 0 (BADR0)
Address offset	10h
Boot-load	FFFFFC00h (1024 bytes in memory space)
Attribute	High bits Read/Write; low bits Read Only
Size	32 bits

Base Address Register 1-5 (BADR1-BADR5)

Register name	Base Address 1-5 (BADR1-BADR5)
Address offset	14h, 18h, 1Ch, 20h, 24h
Boot-load	00000000h (disabled)
Attribute	High bits Read/Write; low bits Read Only
Size	32 bits

CardBus CIS Pointer

Register name	CardBus CIS Pointer
Address offset	28h
Boot-load	00000000h
Attribute	Read Only
Size	32 bits

Subsystem Vendor ID

Register name	Subsystem Vendor ID
Address offset	2Ch
Boot-load	0000h
Attribute	Read Only
Size	16 bits

Subsystem Device ID

Register name	Subsystem Device ID
Address offset	2Eh
Boot-load	see table below
Attribute	Read Only
Size	16 bits

Subsystem Device ID	Value
00h	32-bit S-LINK LDC connector
01h	64-bit S-LINK LDC connector
02h	Single ODIN LDC integrated
03h	Double ODIN LDC integrated

Expansion ROM Base Address Register (XROM)

Register name	Expansion ROM Base Address (XROM)
Address offset	30h
Boot-load	00000000h (disabled)
Attribute	bits 31:11, bit 0 Read/Write; bits 10:1 Read Only
Size	32 bits

Capabilities Pointer

Register name	Capabilities Pointer
Address offset	34h
Boot-load	00h
Attribute	Read Only
Size	8 bits

Interrupt Line Register (INTLN)

Register name	Interrupt Line (INTLN)
Address offset	3Ch
Boot-load	FFh (unknown)
Attribute	Read/Write
Size	8 bits

Interrupt Pin Register (INTPIN)

Register name	Interrupt Pin (INTPIN)
Address offset	3Dh
Boot-load	01h (INTA#)
Attribute	Read Only (RO)
Size	8 bits

Minimum Grant Register (MINGNT)

Register name	Minimum Grant (MINGNT)
Address offset	3Eh
Boot-load	00h (no stringent requirement)
Attribute	Read Only (RO)
Size	8 bits

Maximum Latency Register (MAXLAT)

Register name	Maximum Latency (MAXLAT)
Address offset	3Fh
Boot-load	00h (no stringent requirement)
Attribute	Read Only (RO)
Size	8 bits

Operation Registers

The PCI operation registers are used to operate the interface. The following section describes how the operation registers are used in the interface.

Memory map

The operation registers are mapped into the PCI Memory Space, the base address of which can be found in the PCI Configuration Space in Base Address Register 0. The interface occupies 1 KByte in Memory Space. There are no registers located in the PCI I/O Space.

You can access the registers with 32-bit or with 64-bit PCI cycles. Note that the Request FIFO and Acknowledge FIFO are mapped to multiple addresses. This is done so that multiple accesses can be made by using PCI burst cycles.

Register	Address offset
Operation Control	000h
Operation Status	004h
Interrupt Mask	008h
Test Input	00Ch
reserved	010-0FCh
Request FIFO - Address	1X0h
Request FIFO - Length	1X4h
Request FIFO - Address	1X8h
Request FIFO - Length	1XCh
Acknowledge FIFO - Start control	2X0h
Acknowledge FIFO - End control	2X4h
Acknowledge FIFO - Length	2X8h
reserved	2XCh
reserved	300h-3FCh

Operation Control Register (OPCTL)

Register name	Operation Control register (OPCTL)
Address offset	000h
Boot-load	00000000h
Attribute	Read/Write
Size	32 bits

Bit 31-24	reserved, write as 0
Bit 23	URL3
Bit 22	URL2
Bit 21	URL1
Bit 20	URL0
Bit 19	UDW1
Bit 18	UDW0 [UDW1,UDW0] values: [00]=32-bit [01]=16-bit [10]=8-bit [11]=reserved
Bit 17	URESET 0=normal operation 1=reset S-LINK link card See protocol with LDOWN# Note that this bit is inverted from the signal to the S-LINK
Bit 16	UTDO 0=test data not output to interface 1=test data output to interface Note that this bit is inverted from the signal to the S-LINK
Bit 15-6	reserved, write as 0
Bit 5	TSTCTL: Test mode UCTL 0=test input is data word 1=test input is control word Note that this bit is inverted from the signal to the S-LINK. This bit is used only when the interface is in testmode (when TSTMODE set to 1).
Bit 4	TSTMODE: testmode 0=normal operation 1=take data from Test Input Register (for testing purposes only)

Bit 3	STOP_REQ 0=normal operation 1=stop data transfer Used only for datastreams without control words
Bit 2	SWAP_WORD 0=no swap of 32-bit data words 1=swap of 32-bit data words E.g. 0xAABBCCDD_EEFF0011 becomes 0xEEFF0011_AABBCCDD
Bit 1	SWAP_BYTE 0=no byte swap of data words 1=byte swap of all data words E.g. 0x11223344 becomes 0x44332211
Bit 0	RESET_IF 0=normal operation 1=reset interface

Description

Bits 20 to 23, 18 and 19 of this register are connected to the User Return Line pins and User Data Width pins respectively of the S-LINK interface and have the functionality as described in the S-LINK specification.

Bit 17 is the URESET signal which is used to reset the S-LINK interface. Note that the value in this bit has the inverted level of the signal to the S-LINK. To reset an S-LINK card, the sequence as described in the S-LINK specification has to be followed with the LDOWN# signal. The status of LDOWN# can be read in the Operation Status Register.

Bit 16 is connected to the UTDO# line of the S-LINK interface. Note that the value in this bit has the inverted level of the signal to the S-LINK.

Bits 4 and 5 are used for testing purposes only. If bit 4 is set, the interface will take data from the Test Input Register (TSTIN) instead of the regular S-LINK input. If bit 5 is set, the test words will be received as S-LINK control words, otherwise they are seen as S-LINK data words.

Bit 3, STOP_REQ is only needed for applications that do not use control words in the datastream. In that case the bit is used to let the interface flush its internal buffers to the host memory. When the STOP_REQ bit is set, the interface will assert the UXOFF# signal to the LDC, which prevents new data to come over the link. After 2 µs (which is enough to ‘empty’ a link of up to 150 m), the interface starts dumping all data residing in its internal buffers and will update the ACKFIFO and update the STOP_ACK bit in the Operation Status Register accordingly. When this is finished, the UXOFF# signal will be deasserted again.

STOP_REQ should only be used by data acquisition systems that use no control words and that take data on a burst by burst basis. Here the STOP_REQ bit should be set at the end of a burst to flush the data. When STOP_ACK is set, the interface can be prepared for the next burst of data by resetting the STOP_REQ bit to 0. If STOP_REQ is set before any data came in, the interface will disable itself and no data will be transferred.

Applications that use control words in the datastream (which is the recommended way of using S-LINK as only that way link error detection information will be available), should always have the STOP_REQ bit set to 0 as all data automatically will be transferred to host memory when an ending control word is received.

When bit 2 (SWAP_WORD) is set, the two 32-bit words in all received data words will be swapped. E.g. data received as 0xAABBCCDD_EEFF0011 becomes 0xEEFF0011_AABBCCDD. When set, the swap will be made only on data words. Control words will not be swapped.

When bit 1 (SWAP_BYTE) is set, the bytes in all received data words will be swapped so that words received in little endian format will be transformed into big endian or vice versa. E.g. the received word 0x11223344 becomes 0x44332211. When set, the swap will be made only on data words. Control words will not be swapped.

Bit 0, RESET_IF will reset the complete interface. It will reset all internal FIFOs, state machines and the DMA engine. After writing a 1 to this register, it may take up to one microsecond before the interface is operational again. To operate, the bit has to be reset to 0. To reset the interface it is possible to write a 1, immediately followed by a write of a 0.

Operation Status Register (OPSTAT)

Register name	Operation Status register (OPSTAT)
Address offset	004h
Attribute	Read Only (RO)
Size	32 bits

Bit 31-26	INP_AVAILABLE Shows current number of 64-bit datawords in the Input Buffer FIFO. Six least significant bits only. (for testing purposes only)
Bit 25-20	BURST_AVAILABLE Shows current number of 64-bit datawords in the PCI Burst FIFO. Six least significant bits only. (for testing purposes only)
Bit 19	UXOFF 0=normal S-LINK activity 1=S-LINK transfer has been suspended since last read of the OPSTAT register. Note that this bit is inverted from the signal to the S-LINK. Bit is reset automatically after read of the OPSTAT register.
Bit 18	OVFLW 0=normal S-LINK activity 1=overflow occurred since last read of the OPSTAT register. Bit is reset automatically after read of the OPSTAT register.
Bit 17	LDOWN 0=link is up 1=link is down Note that this bit is inverted from the signal to the S-LINK
Bit 16	STOP_ACK 0=normal operation 1=interface stopped Acknowledge of STOP_REQ in OPCTL, bit reset when STOP_REQ is reset.
Bit 15-12	reserved, ignore value
Bit 11-8	ACK_AVAILABLE Number of blocks that can be read from the Acknowledge FIFO
Bit 7-4	reserved, ignore value
Bit 3-0	REQ_AVAILABLE Number of blocks that can be written to the Request FIFO

Description

The INP_AVAILABLE field is used for testing purposes only. It shows the six least significant bits of the actual number of 66-bit words in the Input Buffer FIFO. As there is other internal storage than the Input Buffer FIFO and the PCI Burst FIFO, the contents of the INP_AVAILABLE field may be different than expected.

The BURST_AVAILABLE field is used for testing purposes only. It shows the six least significant bits of the actual number of 64-bit words in the PCI Burst FIFO. As there is other internal storage than the Input Buffer FIFO and the PCI Burst FIFO, the contents of the BURST_AVALAIBLE field may be different than expected.

Bit 19 (UXOFF) shows that the S-LINK flow control signal UXOFF# has been active since last read of the Operation Status Register. I.e. the data transfer has been suspended for a period of time because the interface could not move the data fast enough out of its internal buffers to the main memory. E.g. the PCI-bus was used by other masters, there were no outstanding REQ_FIFO entries or the ACK_FIFO was full. Once set, the bit will be reset automatically after the read of the Operation Status Register. There is no possibility to read the actual state of the UXOFF signal. When UXOFF has been active, it only means that the data transfer has temporary been interrupted, but no data will be lost because of this.

Bit 18 (OVFLW) will be set when the internal input buffer FIFO is overflown. This may only happen when a simplex LDC is connected to the interface and data is received faster by the LDC than the interface can handle. When a duplex LDC is used, the flow control mechanism will prevent the input buffer FIFO from overflowing. When bit 18 is set, the interface will continue to work, but data may be lost. Once set, the bit will be reset automatically after the read of the Operation Status Register.

Bit 17 shows the current state of the LDOWN# line on the S-LINK connector. Note that the level of this bit is the inverted one of the LDOWN# signal of the S-LINK.

Bit 16, STOP_ACK is used to acknowledge to the user that the interface has actually finished the last transfer as requested by the STOP_REQ bit in the Operation Control Register.

The ACK_AVAILABLE bits give a total count of the number of entries that are available to read from the Acknowledge FIFO. E.g. if the number is three, up to three entries may be read.

The REQ_AVAILABLE bits give a total count of the number of entries that may be written to the Request FIFO before it will be filled. E.g. if the number is three, up to three entries may be written.

Interrupt Mask Register (INTMASK)

Register name	Interrupt Mask register (INTMASK)
Address offset	008h
Boot-load	00000000h
Attribute	Read/Write
Size	32 bits

Bit 31-20	reserved, write as 0
Bit 19	UXOFF 1=interrupt when UXOFF is 1
Bit 18	OVFLW 1=interrupt when FIFO is overflown
Bit 17	LDOWN 1=interrupt when the link went down
Bit 16	STOP_ACK 1=interrupt when STOP_ACK is 1
Bit 15-12	reserved, write as 0
Bit 11-8	ACK_AVAILABLE Interrupt when ACK_AVAILABLE in the Operation Status Register is greater than or equal to this number. A value of 0 means interrupts are disabled.
Bit 7-4	reserved, write as 0
Bit 3-0	REQ_AVAILABLE Interrupt when REQ_AVAILABLE in the Operation Status Register is greater than or equal to this number. A value of 0 means interrupt are disabled.

Description

The Interrupt Mask Register is used to enable interrupts on certain events in the Operation Status Register. If a bit in the Interrupt Mask is set to 1, and the corresponding bit in the Operation Status Register is set to 1, a PCI interrupt will be generated. The interrupt will stay active until the reason for the interrupt has been removed.

The ACK_AVAILABLE field is used to generate an interrupt when there are an equal number or more Acknowledge FIFO entries available than the value of ACK_AVAILABLE. E.g. when ACK_AVAILABLE in the Interrupt Mask Register is set to two, an interrupt will be generated when data is received that generated two or more entries in the Acknowledge FIFO. When set to one, it will generate an interrupt when one or more S-LINK blocks have been received. Note that as long as enough filled Request FIFO entries are still available and the Acknowledge FIFO is not full, the interface will continue to receive data without needing an immediate intervention from the driver. A value of zero will disable the interrupts on the ACK_AVAILABLE field.

The REQ_AVAILABLE field is used to generate an interrupt when there is space available in the Request FIFO for an equal number or more entries than the value of REQ_AVAILABLE. E.g. when REQ_AVAILABLE in the Interrupt Mask Register is set to two, an interrupt will be generated when the user may write two or entries to the Request FIFO. When set to one, it will generate an interrupt whenever at least one Request entry may be written. Note that as long as there are still filled Request FIFO entries available and the Acknowledge FIFO is not full, the interface will continue to receive data without needing an immediate intervention from the driver. A value of zero will disable the interrupts on the REQ_AVAILABLE field.

Test Input Register (TSTIN)

Register name	Test input register (TSTIN)
Address offset	00Ch
Attribute	Write Only
Size	32 bits

Bit 31-0	User Data

Description

This register is used for testing purposes only.

If enabled in the Operation Control Register by bit 4 (TSTMODE), a write to the TSTIN register will behave as if a single S-LINK word has been received with that contents. The type of word (control or data) is determined by bit 5 (TSTCTL) in the Operation Control Register.

Request FIFO (REQFIFO)

Register name	Request FIFO (REQFIFO)
Address offset	1X0h or 1X8
Attribute	Write Only
Size	64 bits

Bit 63-56	reserved, write as 0
Bit 55-32	MAX_BLOCK_LENGTH Maximum Block Length in 32-bit words. Must be a multiple of two. 24 bits, i.e. max. length is 16 MWord -2 or 64 MB -2.
Bit 31-0	START_ADDRESS Start Address. Must be on a 64-bit address boundary.

Description

The Request FIFO is used to tell the interface where to store the data received from the S-LINK. When it receives data, it will put the received start control word in the Acknowledge FIFO and the data in the host memory starting from the Start Address. Data will be transferred to the host memory until either a second control word is received or that the Maximum Block Length is reached. If a second control word is received before the Maximum Block Length is reached, the control word and the length of the received block are put in the Acknowledge FIFO. If the Maximum Block Length is reached before receiving a control word, the data that follows will be put in the memory starting from the Start Address from the next Request FIFO entry.

The Operation Status Register will show the current number of entries in the Acknowledge FIFO. The Maximum Block Length must be a multiple of 8 bytes, i.e. bit 32 of the Request FIFO entry must be 0. The Maximum Block Length includes only the count of data words and does not include the control words. The Start Address must be on a 64-bit address boundary.

Request FIFO entries are handled in the order that they are written to the FIFO. The interface will continue to receive data until all requests are handled, or that the Acknowledge FIFO is full, or that the Stop Request bit in the Operation Control register is set.

Before writing to the Request FIFO address, you should check the REQ_AVAILABLE field in the Operation Status Register to verify that there is still space available or else requests may be lost. In total up to fifteen receive requests may be outstanding. Instead of a single 64-bit write, you may write two 32-bit words to this address. In that case the low address has to be written first (offset 1X0h or 1X8, Start Address), and after that the high address (offset 1X4h or 1XC, Maximum Block Length).

The Request FIFO is mapped to multiple consecutive addresses. This is done so that you may fill up to fifteen locations in the Request FIFO using a single PCI burst write. Be careful to read first from the Operation Status Register how many locations are still available before doing a burst write.

Acknowledge FIFO (ACKFIFO)

Register name	Acknowledge FIFO (ACKFIFO)
Address offset	2X0h
Attribute	Read Only
Size	128 bits

Bit 127-96	reserved, ignore value
Bit 95-63	RX_BLOCK_LENGTH Received Block Length in 32-bit words
Bit 63-35	E_CNTL_H End Control Word contents
Bit 34	E_CNTL_NPRSNT End Control Word not present 0: End control word present 1: End control word not present. I.e. the Maximum Transfer Length as set in the Request FIFO was reached. Ignore control word contents.
Bit 33-32	E_CNTL_L End Control Word contents (contains S-LINK error detection information) When read as 1, those bits have the following meaning: bit 1: transmission error in control word bit 0: transmission error in previous data block.
Bit 31-3	S_CNTL_H Start Control Word contents
Bit 2	S_CNTL_NPRSNT Start Control Word not present 0: Start control word present 1: Start control word not present. I.e. the transfer started without a control word. Ignore control word contents.
Bit 1-0	S_CNTL_L Start Control Word contents (contains S-LINK error detection information). When read as 1, those bits have the following meaning: bit 1: transmission error in control word bit 0: transmission error in previous data block.

Description

The interface writes to the Acknowledge FIFO whenever an S-LINK block of data is received. Normally data is sent in between two control words:

Start control word
Data
End control word

The interface will store the control words that encapsulate the S-LINK data and the length of the received block in the Acknowledge FIFO. If the starting or ending control word is not present, it will be marked in bit 2 of the respective control word (this bit is reserved in the S-LINK specification). The actual data is stored in the host memory starting from the address as it was given by the first available entry in the Request FIFO. Entries in the Request FIFO will be handled on a First In, First Out basis.

The Acknowledge FIFO is effectively 128-bits wide. It may be accessed by two 64-bit reads, in which case a read at the address offset 2X0h will return the Start Control word and the End Control word. The second 64-bit read at address offset 2X8h will return the Received Block Length and will make the next Acknowledge FIFO entry available. You may also read the Acknowledge FIFO with three 32-bit reads on three consecutive addresses. Note that in that case the reserved data (bit 127-96) should not be read as also in this case the read at address offset 2X8h will make the next Acknowledge FIFO entry available.

The received number of S-LINK words is counted in 32-bit word quantities. Although the maximum block length value in the Request FIFO must be an even number of 32-bit words, the interface can receive an odd number of 32-bit S-LINK words and will correctly show the number in the RX_BLOCK_LENGTH field. The Received Block Length field is 32 bits wide, but its value will never exceed the one set in the Request FIFO Maximum Transfer Length field which is 24 bits wide.

The Acknowledge FIFO is mapped on multiple addresses. This is done so you may read up to fifteen locations of the Acknowledge FIFO using a single PCI burst read. Be careful to read first from the ACK_AVAILABLE field in the Operation Status Register how many locations are available to read.

The interface ignores the value of the LDERR# signal of S-LINK, which can be done as every type of S-LINK makes the error detection information also available in the two least significant bits of control words. For applications that would use S-LINK data words only and no control words, there is no possibility to receive link error detection information. Therefore the use of data formats without control words is strongly discouraged.

The following examples show the contents of the Acknowledge FIFO for five possible cases: the block of data received is smaller, the same size, up to twice the size, exactly twice the size and more than twice the size of MAX_BLOCK_LENGTH that was set in the Request FIFO.

In the cases that the size of a block is exactly the same as requested in the Request FIFO or a multiple of it, the end control word will be put in a separate Acknowledge FIFO entry with the RX_BLOCK_LENGTH set to 0. The reason for this is that the interface will already fill the Acknowledge FIFO when the requested amount of data is received. It will not wait for the end control word. In fact those cases are similar to the ones where the amount of received data did not fit in a single entry, but just with 0 extra data words received. Therefore the driver software should not have to consider those as special cases.

Example 1: reception of a 1000 32-bit words packet encapsulated in between control words, with MAX_BLOCK_LENGTH set to 1024 for all Request FIFO entries

RX_BLOCK_LENGTH	1000
END CONTROL	received end control word
START CONTROL	received start control word

Example 2: reception of a 1024 32-bit words packet encapsulated in between control words, with MAX_BLOCK_LENGTH set to 1024 for all Request FIFO entries. In this case two Request FIFO entries are used

RX_BLOCK_LENGTH	1024
END CONTROL	not present
START CONTROL	received start control word
RX_BLOCK_LENGTH	0
END CONTROL	received end control word
START CONTROL	not present

Example 3: reception of a 2000 32-bit words packet encapsulated in between control words, with MAX_BLOCK_LENGTH set to 1024 for all Request FIFO entries

RX_BLOCK_LENGTH	1024
END CONTROL	not present
START CONTROL	received start control word
RX_BLOCK_LENGTH	976
END CONTROL	received end control word
START CONTROL	not present

Example 4: reception of a 2048 32-bit words packet encapsulated in between control words, with MAX_BLOCK_LENGTH set to 1024 for all Request FIFO entries. In this case three Request FIFO entries are used

RX_BLOCK_LENGTH	1024
END CONTROL	not present
START CONTROL	received start control word
RX_BLOCK_LENGTH	1024
END CONTROL	not present
START CONTROL	not present
RX_BLOCK_LENGTH	0
END CONTROL	received end control word
START CONTROL	not present

Example 5: reception of a 2100 32-bit words packet encapsulated in between control words, with MAX_BLOCK_LENGTH set to 1024 for all Request FIFO entries

RX_BLOCK_LENGTH	1024
END CONTROL	not present
START CONTROL	received start control word
RX_BLOCK_LENGTH	1024
END CONTROL	not present
START CONTROL	not present
RX_BLOCK_LENGTH	52
END CONTROL	received end control word
START CONTROL	not present