ATLAS Readout Link

Recommendations of the
Detector Interface Group
ROD Working Group*

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1. INTRODUCTION

The ATLAS management decided in May 2001 to organise the Detector Interface Group (DIG) within the Electronics and Signal Processing activity of the new Technical Coordination structure. The Readout Driver Working Group (ROD WG) is part of the DIG. During the July 2001 T/DAQ week the ROD WG was asked to provide recommendations concerning the Readout Link after which it has set up a Task Force to produce draft recommendations.

The mandate of the Task Force is:

> Bearing in mind the ATLAS requirements, current investments (in money and manpower), testability, maintainability and with the aim of minimising the total cost (avoid local savings) of the ROD/ROL/ROB system in the medium and long term (allow future-proofing), the Task Force should recommend the protocol and the physical implementation of the ATLAS Readout Link.

The members of the Task Force are: Erik van der Bij (chair), Bill Cleland, Philippe Farthouat, David Francis, Andy Lankford, Mike Levine, Robert McLaren and Ralf Spiwoks.

After describing the requirements for the Readout Link and the RODs and ROBs that interface to it, this document will discuss the various aspects for the different options of the links. Finally, the document gives the recommendations that are reported to the ROD WG.

2. SUMMARY OF ATLAS REQUIREMENTS

2.1 Sub-detector RODs

Based on the ATLAS High-level Triggers, DAQ and DCS Technical Proposal [1], the different sub-detectors need in total around 1500 Readout Links. The LArg detector is the largest user with 794 links, followed by the TRT and MDT that need each in the order of 200 links. The maximum throughput required is 160 MByte/s when running at a Level 1 trigger rate of 100 KHz. To reduce the number of types of links, we will consider in this document only Readout Links that can provide this throughput.

The TileCal and LArg detectors need to make the final decision of the Readout Link architecture by the end of the year 2001. Other detectors have similar timescales.

In addition to the links from the RODs to the ROBs, also links from the LVL1 RODs to the Trigger Supervisor are needed. It is foreseen that the same type of link is used as only less than ten of those are needed.

2.2 T/DAQ

The ATLAS High-level Triggers, DAQ and DCS Technical Proposal describes the function and the user requirements of the Readout Link (ROL):

> The principal use of the Readout Link is to connect the RODs to the ROBs. However, other areas of the HLT/DAQ system, for example the LVL1/LVL2 interface, are planning to use the same link since it meets the requirements and a separate development is not justified. Ref. [2] details the advantages of having common ROD outputs and ROLs for all subdetectors.
>
> During the 1998 ROD workshop the user requirements of the ROLs were refined. They can be summarized as:
>
> - Data width and rate: 32 bits at a maximum of 40.08 MHz (i.e. LHC bunch-crossing rate).
> - Control bit to identify start and end of event.
> - Xon/Xoff flow control.
> - Error detection.
> - Error rate < 10^{-12}
> - Maximum length: 300 m for optical version, 25 m for electrical version.

Furthermore T/DAQ requires that the choice of ROL protocol and physical layer should not enforce custom (in-house) developments in the T/DAQ.

3. PRESENT STATUS

3.1 Existing recommendations and documentation

The following documents that relate to the Readout Link are taken into consideration by the Task Force:

- ATLAS High-level Triggers, DAQ and DCS Technical Proposal [1]
- Trigger & DAQ Interfaces with Front-End Systems: Requirement Document [2]
- The Event Format in the ATLAS DAQ/EF Prototype -1 [3]
- ATLAS ROB: User Requirements Document [4]
- Detector and Read-Out Specification, and Buffer-RoI Relations, for Level-2 Studies [5]
- The S-LINK Interface Specification [6]
- Procedures for Standalone ROD-ROL Testing [7]

3.2 Status of Readout Link designs

A specification for a prototype ROL interface, the S-LINK, was drafted in 1995. This interface specifies the signalling and protocol of each end of a link and recommends a connector and mezzanine card including the mechanical details. The mezzanine concept uses daughter boards which plug on to the ROD or ROB motherboards. Based on this S-LINK specification a family of links and test equipment has been designed and commercialised. The family includes optical links, test modules and interfaces to PCI and PMC buses.

The ODIN design is the third generation optical S-LINK implementation, based on Agilent HDMP-1032/1034 (G-LINK) IC's. Two versions exist: 128 MByte/s (Single ODIN) and 160 MByte/s (Double ODIN), which require two and three fibres respectively.

S-LINK test tools that aid in debugging ROD and ROB designs have been used extensively to evaluate performances of ATLAS hardware and software and to ease integration into testbeams. Interfaces between S-LINK link cards and PCI and PMC buses have successfully been used in the LVL2 Pilot Project, in DAQ/EF-1 and in several testbeams and laboratory setups. Drivers have been written for LynxOS and Linux.

Test procedures that ROD designers should follow before integrating with the DAQ system are documented [7]. Over the last years, ROD and ROB designers have built up knowledge about the S-LINK protocol and its mechanical details. This lowers the risks of design mistakes and facilitates discussions between the different groups.

3.3 Status of ROD designs

All current prototype ROD designs have the ROL implemented as S-LINK mezzanine cards.

The following table shows the different implementation possibilities for the final RODs.

Table 1: ROL location and implementation

	ROL location (TM: transition module)	Possible implementation	Requested as mezzanine	Transition module dedicated to ROL only
Pixel/SCT	TM	mezzanine	yes	no
TRT	ROD	mezzanine	yes	-
LArg	TM	mezzanine or integrated	prefer integrated on TM	yes (4 links)
Tilecal	TM (presently)	mezzanine or integrated	no	no (not presently)
Muon MDT	ROD	mezzanine or integrated	no	-
Muon CSC	TM	mezzanine	yes	no
LVL1 muon RPC	ROD	mezzanine	yes	-
LVL1 muon TGC	ROD	mezzanine	yes	-
LVL1 MUCTPI	ROD	mezzanine	yes	-
LVL1 calo PPr	ROD	mezzanine	yes	-
LVL1 calo CP/JEP	TM	mezzanine or integrated	prefer integrated on TM	yes (4 links)
LVL1 CTP	ROD	mezzanine	yes	-

3.4 Status of ROB designs

Current ROB prototype designs have been made based on the requirements as described in the Technical Proposal and in the ROB User Requirements document. The prototype ROBs use S-LINK mezzanine cards as inputs. The design of a production ready ROB is far from being advanced.

4. LINK TECHNOLOGIES

4.1 Gigabit Ethernet / G-LINK

The current ODIN design, based on Agilent G-LINK (de-)serialisers, uses the same type of fibre-optic transceivers that are used by Gigabit Ethernet, which guarantees a continued availability and lower prices in the future.

Because of the maximum datarate of 1 Gbps (1.25 Gbaud) of Gigabit Ethernet components (which also matches the G-LINKs) two fibres and two (de-)serialisers and optical transceivers are needed to reach the full ROL datarate (40 MHz * 32-bits) of 1.28 Gbps (1.6 Gbaud). An additional, third fibre and serialiser/deserialiser pair is needed for the return channel that implements the Xon/Xoff flow control protocol. Because the multiplicity of components required to reach the full ROL datarate, Gigabit Ethernet components are not cost effective for a ROL implementation.

4.2 2.5 Gbps

2.5 Gbps is a new speed in the Fibre Channel standard and is also used in a 10 Gbps Gigabit Ethernet implementation. Reasonably priced components are available on the market. With those components it is possible to build a ROL that can work with only two fibres which will reduce the cost of the final system and which will make it easier to install. Components for 2.5 Gbps have both the serialiser and the deserialiser integrated in one IC, as opposed to the G-LINK where those functions are in separate ICs.

4.3 Channel link

For short, electrical links, Channel Link components are available. These components do a partial serialisation of the data, so that for example 36 bits of data can be sent over 7 twisted pairs (or 48 bits over 9 pairs). New chips include pre-emphasis, DC-balancing and de-skewing logic. According to the datasheet cables longer than 5 meter can be used. Although not using the same chip set that can be used for the Readout Link, LVDS test setups have shown that with a rate of 480 Mbaud per twisted pair, runs up to 20 meter may be possible [8].

4.4 Power dissipation

Table 2 shows the power consumption of the link components for one side of a link built with different technologies.

Table 2: power consumption of the link components on one link side

	GBE / G-LINK [mW]	**2.5 Gbps [mW]**	**Channel link [mW]**
Serialiser and de-serialiser	1875	360	785 (@40 Mhz)
Fibre-optic transceiver	545	412	0
Total	2420	772	785

5. COST ISSUES

5.1 Locations of ROD and ROB

In the baseline setup of the ATLAS system, the RODs will be located in the underground hall USA15 and the ROBs will be in the surface building called SDX. In this case all 1500 read-out links will be around 170 meter long and patch panels are needed for all those links. Any implementation in which the concentration of the ROB outputs will be done in the surface building, will need this large fibre-optic installation (see appendix A, architectures A-C).

In an implementation where the concentration of the ROB outputs can be done in the underground hall, only 300 (or less, depending on the degree of concentration) 170 meter links are needed to move the data from the underground to the surface (see appendix A, architectures D-F). Such an implementation will create considerable savings in the cable and patch panel installation (see appendix B) which outweighs other optimisations in the ROL.

The decision on the final implementation of the ROD, ROB and concentrator is outside the scope of the ROL task force. We therefore recommend that T/DAQ will set up a separate task force to study this option.

The location of the ROD and ROB does not change the architecture of the ROL. The only difference is the distance between the ROD and the ROB, which may lead to cheaper implementations of the ROL.

5.2 2.5 Gbps vs 1.25 Gbps

Using 2.5 Gbps components one will need only two fibre-optic transceivers for a link instead of four as currently used in the ODIN design. One can calculate from Table 3 that using 2.5 Gbps components one will save 90 CHF per link (in the year 2003) in the fibre-optic transceivers.

Table 3: Price evolution of Infineon fibre-optic transceivers (5K quantity per year) - data provided by Infineon

Date	Price 1.25 Gbps [CHF]	Price 2.5 Gbps [CHF]
Oct 2000 -	130	
Oct 2001 -	104	167
Oct 2002 -	90	133
Oct 2003 -	78	111
Oct 2004 -	66	90
Oct 2005 -	60	78

It is expected that the use of 2.5 Gbps (de-)serialisers can make a difference of about CHF 86 per Readout Link compared to using G-LINK components (2001 prices). In an ODIN link six G-LINK components are needed, while only two 2.5 Gbps (de-)serialisers are needed. In cabling there will be a saving of 33%. It is not only that a third less fibres are needed, but also a third less of patch panels and patch cords.

5.3 2.5 Gbps vs electrical

If the RODs and ROBs can be placed near to each other, it may be possible to use an electrical link. In this case no expensive fibre-optic transceiver is needed. However, the price of electrical halogen-free cables is much higher than fibre-optic cables of the same length.

Table 4 shows a price comparison between the different options of the ROL. The table is based on a production in the year 2003. Refer to appendices C to F for a detailed calculation of the costs of the Link Cards. If the ROBs can handle four inputs, the Electrical Channel Link for the LArg detector can optimise the cable cost as it may share one large cable for four RODs.

Table 4: cost comparison of complete 12 meter Readout Links

	Optical ODIN [CHF]	**Optical 2.5 Gbps [CHF]**	**Electrical Channel Link non-LArg (1 cable/link) [CHF]**	**Electrical Channel Link LArg (1 cable/4 links) [CHF]**
Link Source Card	370	282	141	141
Cable	232	101	240	123
Link Destination Card	370	282	141	141
Total per ROL	972	665	523	405
750 Readout Links			392250	303750
1500 Readout Links	1458000	997500	696000	

5.4 Integration

The approach used until now is to have the ROL on mezzanine cards (mezzanine version). A way to reduce the total cost of a link implementation is to integrate the link design onto the ROD or ROB (integrated version). By integrating the link design, a seperate PCB, front-panel and mezzanine connector are not needed, and the additional fabrication costs are low. This can save around CHF 40 per card (see appendix F).

If we choose a mezzanine solution one may gain by buying the components later as with time prices are expected to fall. Table 3 gives an example of that. As the ROD boards are very complex they will have to be built before mezzanine cards. Therefore if the ROL would be integrated on the ROD, we cannot profit from this price evolution.

6. OTHER ISSUES

6.1 Testability

To allow easy testability, it is recommended that the ROD designs will have testpoints attached to the signals UCLK, UWEN, LFF and UCTRL (LCLK, LWEN, UXOFF, LCTRL on the ROB). Care should be taken to not influence the signal quality of those lines, by either having a passive testpoint in the middle of the signal to the S-LINK connector or by using buffered versions of those signals.

Boards using the S-LINK mezzanine cards will be able to use dedicated S-LINK test tools that allow to view all of the ROL signals.

6.2 Maintainability

When mezzanine cards are used for the ROL, it will be easier to change the ROL in case it is broken. It may mean that less spare complete RODs and ROBs are needed.

As ROL mezzanines are common to all detectors, it is likely that an ATLAS wide set of spare cards will exist, which reduces the total cost.

6.3 Risks

Having a ROL design integrated on the ROD or ROB is a higher risk than if it is implemented as a mezzanine card. In case of an integration, gigabit lines have to be implemented on the board requiring special high-speed design techniques. This will have to be done for all subdetectors that choose for integration. If a mezzanine implementation is chosen, the highest clock speed is 40 MHz, which does not require any special design techniques.

In case the design of the 2.5 Gbps version would have problems (difficulty of obtaining components, engineering or manpower problems), it will be possible to fall back to the proven ODIN design when a mezzanine solution is chosen. Of course in that case the fibre installation must be enlarged as well.

The S-LINK cards use the IEEE 1386 Mezzanine Connector. Connectors may have contact problems. With the experience gained over the past years within the community, we believe that there is a very low risk associated with those connectors if the mezzanine cards are correctly mechanically fixed to the motherboards.

6.4 Schedule

An integrated link implementation would be cheaper than a mezzanine version, but it is impossible to have a new 2.5 Gbps or electrical link design ready before the ROD designers need to finalise their schematics. We estimate that it will take about one manyear to design a new link.

As ROB designs will be made later, it means that if necessary the link designs can be ready for integration with the ROB.

7. ADVANTAGES AND DISADVANTAGES OF POSSIBLE SCENARIOS

7.1 Interface protocol

We currently have working RODs, ROLs and ROBs which share common interfaces across the experiment providing a standard interface to the T/DAQ system. The advantages of having a uniform interface to the detectors is clear. Based on the general acceptance, positive feedback, current investments and on the wide-spread know-how it is important to continue to use this common interface based on the S-LINK specification.

7.2 Integrated or mezzanine

The main decision comes down to the choice between integrating current implementations based on today's technology (integrated version) or recommending a more flexible approach where the ROL is implemented on mezzanine boards (mezzanine version).

The advantages of mezzanines are:

- allows the use of currently existing link mezzanines and test tools
- allows to benefit from future cost reductions
- much easier to design the ROD and the ROB
- allows future upgrades and the feasibility of implementing the ROBs as mezzanine cards located on the RODs (ROB-on-ROD).
- eases repairs
- gives time to design a cheaper link
- allows the possibility to fall back to the baseline ODIN design
- allows the difficult high-speed part to be designed only once

The disadvantages of mezzanines are:

- increases cost. However, a large part of the offset in cost is removed when the mezzanine cards are produced in quantity, produced later than integrated versions and use newer components than the ODIN.
- the mezzanine connector may be unreliable. With the experience we have now, this is not believed to be an issue.

By incorporating into the design of the ROD a transition module dedicated to integrated readout links, one realizes some of the advantages of both the mezzanine solution (buying components later) and the integrated solution (no front panel or mezzanine connector required). However, whereas a fully mezzanine based design can be upgraded by just changing the mezzanine link card, a transition module design with an integrated readout link would need to be replaced by a redesigned transition module.

7.3 Electrical or optical

If the ROD and ROB can be located close to each other, another choice is to be made: should the physical link be electrical or optical?

The major advantage of a fibre-optic implementation over an electrical one is that it can handle all different architectures of the ROD/ROB system as a single design can be used for both short distance and long distance links. Current electrical link designs can be used only for links of up to around 20 m. However, in time this may be increased by new technical solutions to the required 25 m.

If in the final system we would use electrical links for the short distances and optical ones for the long distances, it would mean that two link types have to be designed, manufactured and to be maintained instead of just one. Furthermore, as it is likely that the ROBs will need to integrate the link logic, two different ROB designs will have to be made, manufactured and maintained.

The design cost for the electrical link is estimated at 100 KCHF. The additional maintenance cost (including spares) will be around 30 KCHF. A second ROB design will cost around 50 KCHF as just the link input needs to be redesigned. An additional 30 KCHF is required for ROB maintenance. Therefore, if not all detectors can use an electrical link, the lower cost for the links (around 200 KCHF) will not cover the additional design and maintenance costs.

8. RECOMMENDATIONS OF THE RODWG ROL TASK FORCE

The RODWG Readout Link task force recommends the following:

1. ATLAS Readout Links shall comply with the S-LINK specification

2. ATLAS Readout Links shall be optical

3. A. ROD boards not using a transition module shall be designed to accept S-LINK Mezzanine link cards (3.3 Volt)
   B. ROD boards with a mixed functionality transition module (readout link and other logic) shall design the transition module to accept S-LINK Mezzanine link cards (3.3 Volt)
   C. ROD boards with a transition module dedicated to the readout link may integrate the read-out link logic on the transition module.

4. The ROB should be designed to accept the S-LINK protocol. The physical implementation (mezzanine or integration) is left to the ROB designers

5. A project shall be set up to design an S-LINK mezzanine card using 2.5 Gbps components and requiring only two fibres per Readout Link

Furthermore the task force would like to raise the following issues:

1. ATLAS Technical Coordination should investigate the fibre installation issues (costing, coordination, installation) for all optical links

2. T/DAQ should set up a separate task force to study the location of ROBs and the feasability of the ROB-on-ROD option

9. REFERENCES

[1] ATLAS High-level Triggers, DAQ and DCS Technical Proposal, CERN/LHCC/2000-17, 31 March 2000.

[2] Trigger & DAQ Interfaces with Front-End Systems: Requirement Document http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/DIG/archive/document/FEdoc_2.5.pdf

[3] The event format in the ATLAS DAQ/EF prototype -1, C. Bee et al., 15 October 1998, ATLAS note DAQ-98-129 http://atddoc.cern.ch/Atlas/postscript/Note050.ps

[4] ATLAS ROB: User Requirements Document, O. Boyle et al, 12 January 2000 http://hsi.web.cern.ch/HSI/atlas/rob/

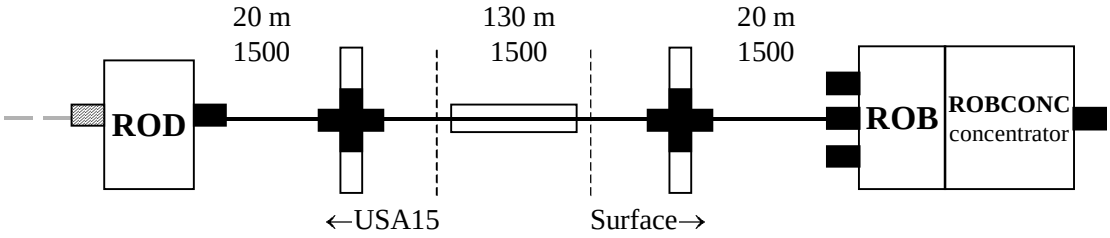
[5] Detector and Read-Out Specification, and Buffer-RoI Relations, for Level-2 Studies, P. Clarke et al., October 1999, ATL-DAQ-99-014 http://documents.cern.ch/cgi-bin/setlink?base=atlnot&categ=Note&id=daq-99-014

[6] The S-LINK Interface Specification, O. Boyle et al, 27 March 1997 http://edmsoraweb.cern.ch:8001/cedar/doc.info?document_id=110828

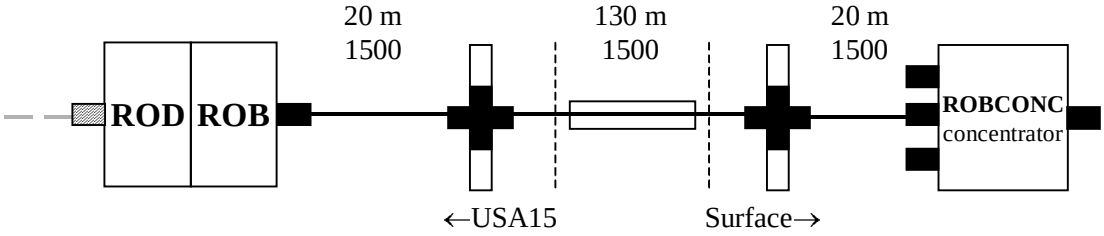
[7] Procedures for Standalone ROD-ROL Testing, G. Lehmann et al. 27 July 2001, ATC-TD-TP-0001 http://edmsoraweb.cern.ch:8001/cedar/doc.info?document_id=320873&version=1

[8] Study of LVDS Serial Links for the ATLAS Level-1 Calorimeter Trigger, G. Anagnostou et.al, September 2000, LEB2000 http://hepwww.rl.ac.uk/Atlas-L1/Publications/2000/leb2000_lvds.pdf

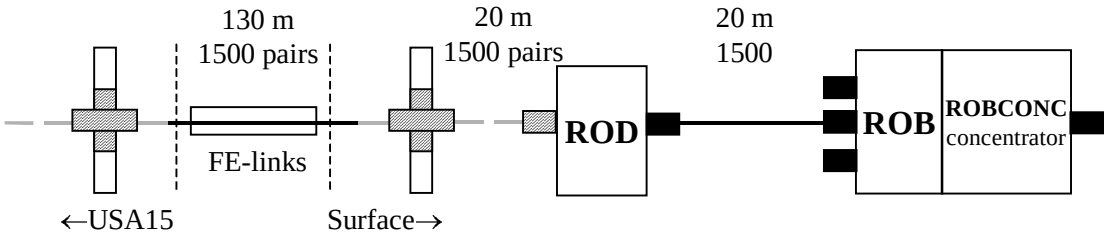
Appendix A. SAMPLE ARCHITECTURES OF THE ROD/ROB SYSTEM



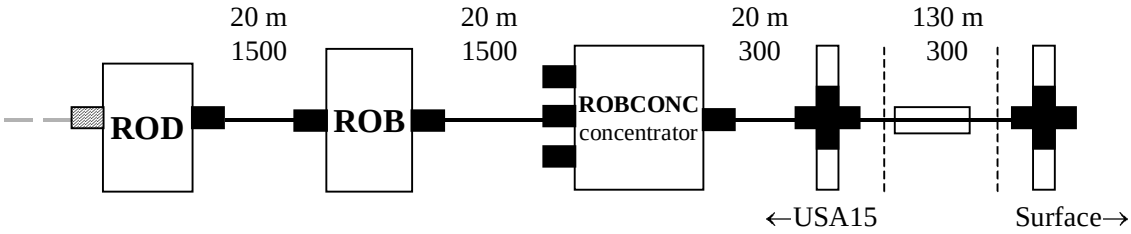
A: Baseline - ROB on surface



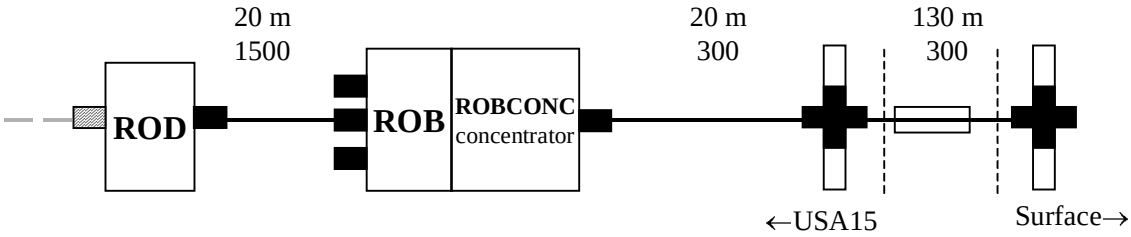
B: ROB-on-ROD - concentrator on surface



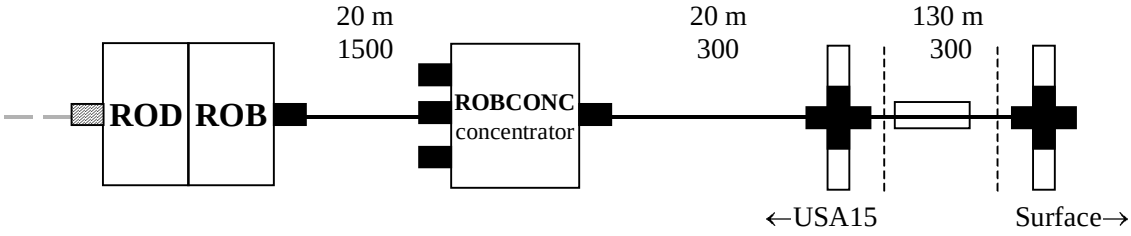
C: ROD, ROB and concentrator on surface
(LArg only. For comparison scaled to same size as full ATLAS; actual LArg installation half the size as shown)



D: ROD, ROB and concentrator underground



E: ROD and multi-input ROB underground



F: ROB-on-ROD and concentrator underground

Appendix B. FIBRE INSTALLATION COST OF SAMPLE ARCHITECTURES

The following table shows a calculation of the fibre installation cost for the sample architectures as shown in Appendix A. Costing is based on a single offer received on 13 November 2001 in which the bulk cable fibre was replaced by a cheaper one (CHF 0.47 vs. CHF 0.10/m per fibre).

	Number	A	B	C	D	E	F
20 m duplex patch cable		3'000	3'000	1'500	3'300	1'800	1'800
130 m bulk cable (pairs)		1'500	1'500	1'500	300	300	300
patch panel (duplex)		3'000	3'000	0	600	600	600
	Price [CHF]						
20 m duplex patch cable	104	312'000	312'000	156'000	343'200	187'200	187'200
130 m bulk cable (/pair)	157	235'500	235'500	39'000	47'100	47'100	47'100
patch panel (/duplex)	26	78'000	78'000	0	15'600	15'600	15'600
installation cost (/bulk cable pair)	46	69'000	69'000	69'000	13'800	13'800	13'800
Total cost [CHF]		694'500	694'500	264'000	419'700	263'700	263'700

Item	Details
Patch cable	duplex patch cord 50/125 um, 20 meter connectorised in factory with duplex LC or compatible connectors on both sides
Bulk cable	cable with 84 seperate fibres 50/125 um 130 meter connectorised in factory with duplex LC or compatible connectors on both sides. Option C: not connectorised cable
Patch panel	built up out of 19", 2HE units with 42 duplex LC or LC compatible adapters

Note 1: this calculation does not take into account the price of the empty patch panel crates (about 25 KCHF) as this is considered to be part of the infrastructure.

Note 2: the price in architecture C does not include the patch panels shown in Appendix A as they are part of the front-end link (the other options will have similar patch panels not shown in the diagrams). The bulk cable (without connectorisation) is included in option C as this is an additional front-end link cost that the other options don't have. With this calculation the architectures shown are comparable.

Appendix C. COST CALCULATION OPTICAL ODIN

Component	Type	Manufacturer	Description	/card	Price/pc	Total
Integrated circuits						
Protocol chip	EP1K30QC208-1	Altera	208-pin PQFP	1	46.00 CHF	46.00 CHF
Configuration EPROM	EPC1441PC8	Altera	8 pin	1	5.00 CHF	5.00 CHF
Low Power G-LINK Tx	HDMP-1032	HP (SEI)		2	31.00 CHF	62.00 CHF
Low Power G-LINK Rx	HDMP-1034	HP (SEI)		1	31.00 CHF	31.00 CHF
SFF optical transceiver LC	V23818-K305-L17	INFINEON	Small form Factor	2	78.00 CHF	156.00 CHF
3.3V/2.5V		Linear Tech.	TO220H	1	5.00 CHF	5.00 CHF
Crystal Oscillator 64 Mhz	F1 SPXO014814 X447T 64MHz IQXO-71 B BU	IQD		1	5.00 CHF	5.00 CHF
Crystal Oscillator 40 Mhz	F1 SPXO003202 X357V 40MHz IQXO-71C BU	IQD		0	3.14 CHF	0.00 CHF
Connectors						
S-LINK connector	120527-1 / CERN SCEM 09.55.40.064.7	AMP	IEEE1386 CMC "P" plug	1	4.26 CHF	4.26 CHF
LEDs						
Green LED	RTE3104G	MENTOR	For Front Panel	2	0.82 CHF	1.64 CHF
Red LED	RTE3104R	MENTOR	For Front Panel	3	0.82 CHF	2.46 CHF
Inductors						
Media intf. Power filter	HF70ACC453215T	TDK	SMD	2	1.00 CHF	2.00 CHF
Other						
EPROM socket	Holtite		DIL, 8 pin	1	0.11 CHF	0.11 CHF
Capacitors						
Bypass capacitors, 100nF	0805			94	0.06 CHF	5.64 CHF
Buffer capacitor, 10uF	B 45196 E 5106-M9		tantalum	12	0.44 CHF	5.28 CHF
Resistors						
68	0805			5	0.01 CHF	0.05 CHF
180	0805			11	0.01 CHF	0.11 CHF
1K	0805			13	0.01 CHF	0.13 CHF
Total						**331.68 CHF**

Appendix D. COST CALCULATION OPTICAL 2.5 GBPS

Component	Type	Manufacturer	Description	/card	Price/pc	Total
Integrated circuits						
Protocol chip	EP1K30QC208-1	Altera	208-pin PQFP	1	46.00 CHF	46.00 CHF
Configuration EPROM	EPC1441PC8	Altera	8 pin	1	5.13 CHF	5.13 CHF
Transceiver	TLK2501	TI		1	48.00 CHF	48.00 CHF
SFF optical transceiver LC	V23818-N305-L57 (2001 price 111 Euro)	INFINEON	SFF 2.5 Gbps	0	167.00 CHF	0.00 CHF
SFF optical transceiver LC	V23818-N305-L57 (2003 price 74 Euro)	INFINEON	SFF 2.5 Gbps	1	111.00 CHF	111.00 CHF
3.3V/2.5V		Linear Tech.	TO220H	1	5.00 CHF	5.00 CHF
Crystal Oscillator 125 Mhz		IQD		1	5.00 CHF	5.00 CHF
Connectors						
S-LINK connector	120527-1 / CERN SCEM 09.55.40.064.7	AMP	IEEE1386 CMC "P" plug	1	4.26 CHF	4.26 CHF
LEDs						
Green LED	RTE3104G	MENTOR	For Front Panel	2	0.82 CHF	1.64 CHF
Red LED	RTE3104R	MENTOR	For Front Panel	3	0.82 CHF	2.46 CHF
Inductors						
Media intf. Power filter	HF70ACC453215T	TDK	SMD	3	1.00 CHF	3.00 CHF
Other						
EPROM socket	Holtite		DIL, 8 pin	1	0.11 CHF	0.11 CHF
Capacitors						
Bypass capacitors, 100nF	0805			94	0.06 CHF	5.64 CHF
Buffer capacitor, 10uF	B 45196 E 5106-M9		tantalum	12	0.44 CHF	5.28 CHF
Resistors						
68	0805			5	0.01 CHF	0.05 CHF
180	0805			11	0.01 CHF	0.11 CHF
1K	0805			13	0.01 CHF	0.13 CHF
Total						**242.81 CHF**

Appendix E. COST CALCULATION ELECTRICAL CHANNEL LINK

Component	Type	Manufacturer	Description	/card	Price/pc	Total
Integrated circuits						
Protocol chip	EP1K30QC208-2	Altera	208-pin PQFP	1	33.52 CHF	33.52 CHF
Configuration EPROM	EPC1441PC8	Altera	8 pin	1	5.13 CHF	5.13 CHF
Serialiser	DS90CR483	National Semiconductor		1	19.00 CHF	19.00 CHF
LVDS Buffer	unknown			1	3.00 CHF	3.00 CHF
Connectors				1	6.90 CHF	6.90 CHF
3.3V/2.5V		Linear Tech.	TO220H	1	5.00 CHF	5.00 CHF
Crystal Oscillator 125 Mhz		IQD		1	6.50 CHF	6.50 CHF
Connectors						
S-LINK connector	120527-1 / CERN SCEM 09.55.40.064.7	AMP	IEEE1386 CMC "P" plug	1	4.26 CHF	4.26 CHF
LEDs						
Green LED	RTE3104G	MENTOR	For Front Panel	2	0.82 CHF	1.64 CHF
Red LED	RTE3104R	MENTOR	For Front Panel	3	0.82 CHF	2.46 CHF
Inductors						
Media intf. Power filter	HF70ACC453215T	TDK	SMD	3	1.00 CHF	3.00 CHF
Other						
EPROM socket	Holtite		DIL, 8 pin	1	0.11 CHF	0.11 CHF
Capacitors						
Bypass capacitors, 100nF	0805			94	0.06 CHF	5.64 CHF
Buffer capacitor, 10uF	B 45196 E 5106-M9		tantalum	12	0.44 CHF	5.28 CHF
Resistors						
68	0805			5	0.01 CHF	0.05 CHF
180	0805			11	0.01 CHF	0.11 CHF
1K	0805			13	0.01 CHF	0.13 CHF
Total						**101.73 CHF**

Appendix F. COST COMPARISON OF MEZZANINE DESIGNS

	Optical ODIN [CHF]	Optical 2.5 Gbps [CHF]	Electrical Channel Link [CHF]
Components	331	243	102
PCB	11	11	11
Front panel	13	13	13
Mounting	15	15	15
Total per side	370	282	141
3000 sides	1110000	846000	423000

Note: costing based on production in the year 2003