The ATLAS ROD Busy Module

ATLAS ROD Workshop

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General:

- There are about 1700 Read Out Driver (ROD) modules in the ATLAS Experiment.
- The ROD's contain data buffers that can fill up.
- A BUSY signal is generated by the ROD when its buffer is nearly filled.
- The BUSY signals are fed to the ROD-BUSY modules, which in turn are connected in a tree structure.
- The SUM of all BUSY signals is flagged as a VETO to the CTP.

Each ROD-BUSY module:

- has 20 BUSY inputs and one BUSY-CARRY-IN input.
- monitors each BUSY input line.
- is able to mask each BUSY input line.
- measures, in numbers of BC, each asserted BUSY line.
- produces the SUM of all BUSY lines, including the BUSY-CARRY-IN input, as a BUSY-OUT signal
- generates a VME interrupt after a programmed time-out.

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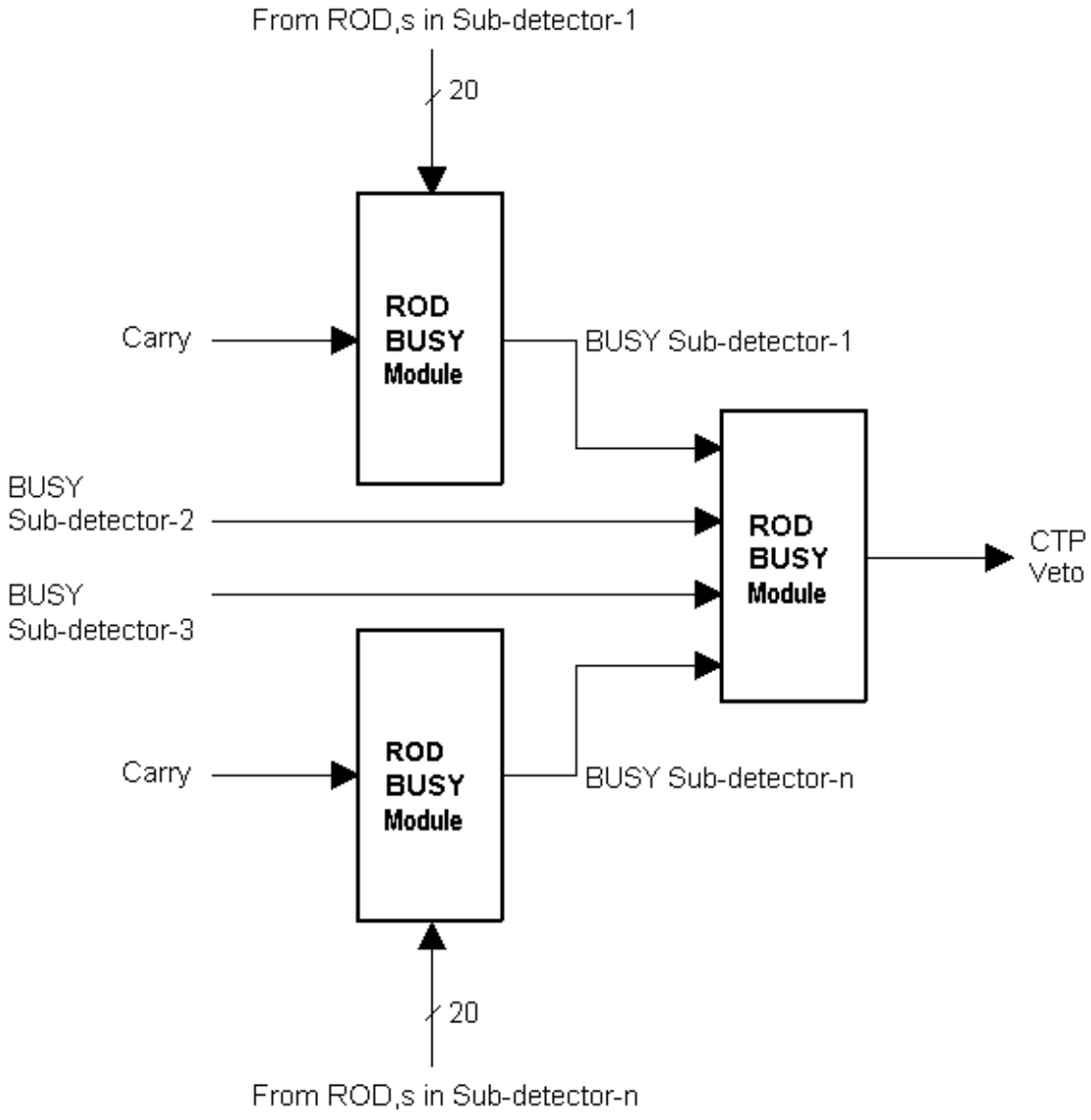
ROD BUSY Module Interchaining



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Preliminary Specification of the ATLAS ROD BUSY Module

Back plane protocol:	VME: A24,A16/D16
Address Modifiers:	Standard: 39, 3A, 3D, 3E Short : 29, 2D Extended: 09, 0A, 0D, 0E (for CPU compatibility)
VME Interrupter:	ROAK type (release on acknowledge), programmable IRQ priority level (1 to 7), programmable STATUS I/D D08(odd) or D16
Configuration ROM:	EEPROM to store manufacturer/board/revision ID
Front panel signal levels:	NIM 50Ω (where TRUE is -16 mA i.e. -0.8V @ 50Ω and FALSE is 0 mA)
Busy inputs:	20 (LEMO® #00) from ROD's
Busy Carry Input:	1 (LEMO® #00) from previous ROD BUSY module
Busy Out:	2 (LEMO® #00) one to next ROD BUSY module, the other for monitoring.
Clock input:	1 (LEMO® #00) BC 40.08 MHz
Clock selection:	Automatic between external and internal (40 MHz)
Busy Duration Monitor:	Max duration: $2^{16} * 1/40 * 10^{6}$ = 1.64 ms, i.e. 16 bit counter at 40 MHz Counter readable via a VME address. Reset by writing 0 to counter or via global reset command.
Power Requirements:	+ 5.0 volt - 5.0 volt (generated internally or from special power bus in ROD crate ??)
Module PCB size:	prototype: 233.4 * 160.0 mm (height * width)
Front panel size:	prototype: 261.9 * 20.0 mm (6U * 4TE)
	A conversion kit is foreseen in order to be compatible with 9U / 400 mm ROD - crates.

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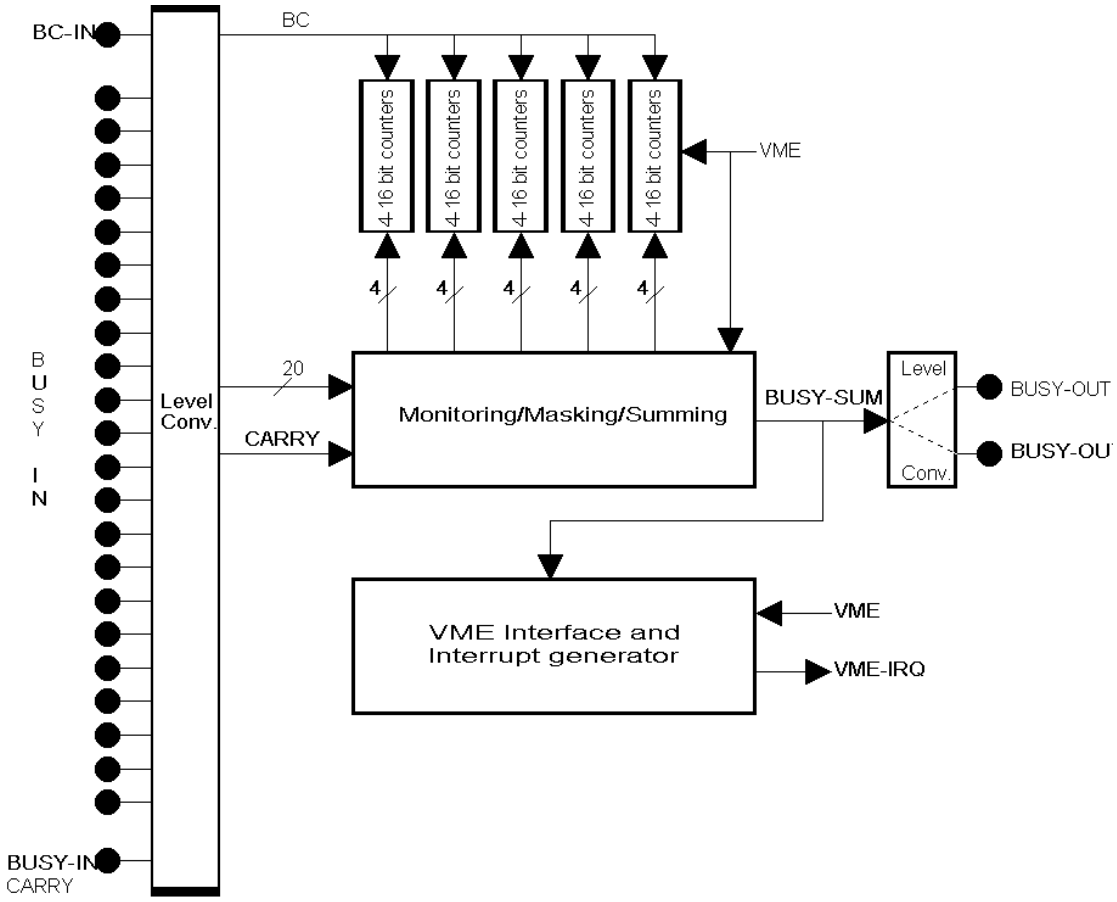
ATLAS ROD BUSY Module Block Diagram



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ROD-BUSY MODULE REGISTER OFFSETS

Addr. offset	Register	R/W	Access	Remarks
CE 1100-1110				
CC 1100-1100				
CA 1100-1010				
C8 1100-1000				
C6 1100-0110	DUR-BUSY-19	R/W	W 16	Busy duration counter 19
C4 1100-0100	DUR-BUSY-18	R/W	W 16	Busy duration counter 18
C2 1100-0010	DUR-BUSY-17	R/W	W 16	Busy duration counter 17
C0 1100-0000	DUR-BUSY-16	R/W	W 16	Busy duration counter 16
BE 1011-1110	DUR-BUSY-15	R/W	W 16	Busy duration counter 15
BC 1011-1100	DUR-BUSY-14	R/W	W 16	Busy duration counter 14
BA 1011-1010	DUR-BUSY-13	R/W	W 16	Busy duration counter 13
B8 1011-1000	DUR-BUSY-12	R/W	W 16	Busy duration counter 12
B6 1011-0110	DUR-BUSY-11	R/W	W 16	Busy duration counter 11
B4 1011-0100	DUR-BUSY-10	R/W	W 16	Busy duration counter 10
B2 1011-0010	DUR-BUSY-9	R/W	W 16	Busy duration counter 9
B0 1011-0000	DUR-BUSY-8	R/W	W 16	Busy duration counter 8
AE 1010-1110	DUR-BUSY-7	R/W	W 16	Busy duration counter 7
AC 1010-1100	DUR-BUSY-6	R/W	W 16	Busy duration counter 6
AA 1010-1010	DUR-BUSY-5	R/W	W 16	Busy duration counter 5
A8 1010-1000	DUR-BUSY-4	R/W	W 16	Busy duration counter 4
A6 1010-0110	DUR-BUSY-3	R/W	W 16	Busy duration counter 3
A4 1010-0100	DUR-BUSY-2	R/W	W 16	Busy duration counter 2
A2 1010-0010	DUR-BUSY-1	R/W	W 16	Busy duration counter 1
A0 1010-0000	DUR-BUSY-0	R/W	W 16	Busy duration counter 0
9E 1001-1110	INT-TO-CMP	R/W	W 16	VME Interrupt Time-out Compare reg
9C 1001-1100	INT-TO-CNT	R/W	W 16	VME Interrupt Time-out Counter
9A 1001-1010	INT-STATUS-ID	R/W	W 16	VME Interrupter Status/ID reg
98 1001-1000	INT-CSR	R/W	W 16	VME Interrupter CSR
96 1001-0110	BUSY-MASK-L	R/W	W 16	SET/CLR Busy/Carry masks LO
94 1001-0100	BUSY-MASK-H	R/W	W 16	SET/CLR Busy/Carry masks HI
92 1001-0010	BUSY-STATE-L	R	W 16	Read state of busy lines after mask LO
90 1001-0000	BUSY-STATE-H	R	W 16	Read state of busy lines after mask HI
8E 1000-1110				
8C 1000-1100				
8A 1000-1010				
88 1000-1000				
86 1000-0110	SW-RST-CNT	W	W -	Reset all counters / data-less function
84 1000-0100	SW-RST	W	W -	Reset module / data-less function
82 1000-0010				
80 1000-0000	CSR	R/W	W 16	see bit map
00 0000-0000	Conf. EEPROM	R/(W)	W 8	LSBytes in every Long Word. See specs.

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CONFIGURATION - IDENTIFICATION EEPROM MAPPING

VME Address Offsets					
MSBYTE			LSBYTE		
31 24	23 16	15 8	7 0		
20	21	22	23		
24	25	26	27	Manufacturer ID (CERN)	MSBYTE
28	29	2A	2B	Manufacturer ID (CERN)	
2C	2D	2E	2F	Manufacturer ID (CERN)	LSBYTE
30	31	32	33	Board ID / Serial No.	MSBYTE
34	35	36	37	Board ID / Serial No.	
38	39	3A	3B	Board ID / Serial No.	
3C	3D	3E	3F	Board ID / Serial No.	
40	41	42	43	Board Revision No.	MSBYTE
44	45	46	47	Board Revision No.	
48	49	4A	4B	Board Revision No.	
4C	4D	4E	4F	Board Revision No.	LSBYTE

The IEEE Manufacturer ID# for CERN is: 080030 (hex)

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