Procedures for Standalone ROD-ROL Testing

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Abstract

This note describes the series of tests which should be performed by ROD developers to assure the correct flow of event data towards the DAQ system over the ReadOut Link, prior to integrating with the TDAQ system.

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1 Introduction

The scope of this document is to provide guidelines to achieve an efficient and smooth integration between the RODs and the TDAQ system. In particular it focuses on the ReadOut Link (ROL), which connects the RODs to the ReadOut Subsystem (ROS). This link is used to send event data which have been accepted by the first level Trigger to the DataFlow system. The ROL implementation is based on the S-LINK specification [1].

Section 2 describes a series of tests which shall be performed by ROD developers to assure the proper flow of event data towards the DAQ system over the S-LINK protocol, prior to integrating with the TDAQ system. The tests focus in particular on the flow control features of the S-LINK and on the way the S-LINK should be reset, since these two aspects have shown[1] to be error prone.

The appendices to this document provide supporting information to the ROD designers. Appendix A recalls the main features of S-LINK and their usage, Appendix B lists the debugging facilities for S-LINK and Appendix C describes the data format for the ROD data, as extracted from [2].

2 Tests

In this section a series of tests is described, which shall be executed on the RODs to test their S-LINK interface. The outcome of these tests should be documented and ready for discussion when starting to plan the integration of the ROD with the TDAQ system.

2.1 Test Items

During the design phase of a ROD it should be assured that the functional requirements listed below are fulfilled. These requirements form also the test items that have to be verified before integration with the TDAQ system. For all ROD implementations which have an S-LINK connector[2] the procedures to check the fulfillment of the requirements are presented in Section 2.2.

1. The ROD shall be able to send out data over S-LINK.
2. The ROD shall be able to reset the S-LINK. The RESET of the Link Source Card (LSC) shall follow the protocol between URESET# and LDOWN# as specified in the S-LINK specification ([1], section 4.11).
3. The ROD shall implement the LFF# flow control. After the LSC has asserted an LFF# low, the ROD shall never send more than two (2) words to the LSC with UWEN# low, as specified by the S-LINK specification([1], section 4.6).
4. The ROD shall send out data according to the Event Format specification [2].

1. We refer here to the experience gained during the integration of the CPROD, LArROD and MIROD with the ROS.

2. It is recommended to use the ROL mezzanine cards on the ROD and not to integrate the ROL circuitry directly on the ROD PCB [3].

2.2 Test Procedures

1. Test of the basic S-LINK functionality

   a) Mount a SLIDAD (see Appendix B) on the ROD instead of the LSC card.

   b) Program the ROD to send out one word at a time (possibly a walking bit).

   c) Verify the correct arrival of the data with the SLIDAD LEDs.

2. Test of the reset protocol

   a) Mount a SLIDAD on the ROD instead of the LSC card.

   b) Put SW1 of the SLIDAD in position 0 (Run).

   c) The URESET# and LDOWN# LEDs on the SLIDAD should be off.

   d) Let the ROD give a reset of the SLIDAD.

   e) The URESET# and LDOWN# LEDs on the SLIDAD should still be off (the reset goes too fast for the eye to see).

   f) Now put SW1 of the SLIDAD in position 1 (Single Step).

   g) The URESET# and LDOWN# LEDs on the SLIDAD should be off.

   h) Let the ROD give a reset to the SLIDAD.

   i) The URESET# and LDOWN# LEDs on the SLIDAD should be on.

   j) Press the STEP button.

   k) The URESET# and LDOWN# LEDs on the SLIDAD should be off.

   l) *Optional:* Check with a logic state analyzer that the waveforms comply to the S-LINK specification([1], section 4.11).

3. Test of the Flow Control

   a) Mount a SLIDAD on the ROD instead of the LSC card.

   b) Put SW1 of the SLIDAD in position 0 (Run).

   c) Let the ROD send data continuously.

   d) The UWEN# LED should light up.

   e) Program the ROD to send a known data pattern, such as an incrementing number.

   f) Put SW1 of the SLIDAD in position 1 (Single Step).

   g) Let the ROD send data continuously.

   h) The UWEN# LED should be off, the LFF LED should be on.

   i) Press the STEP button.

   j) Look at the data LEDs of the SLIDAD and check if at maximum three words have been transfered. If the flow control is implemented correctly, the first word will make LFF# go to 0, and then the ROD may transfer at maximum two extra words.

   k) Go to step i).

l) *Optional:* ROD designers are encouraged to do a long duration test by testing the flow control with a Logic State Analyzer connected to the SLIDAD that checks the amount of words in each event. A pulse generator connected to the SLIDAD can emulate the flow control.

4. Data Format Verification

a) Setup a PC with an S-LINK receiver card[1].

b) Install the PC with the proper operating system, drivers and DataFlow software[8].

c) Program the ROD to send always the same event (test-event), with the exception of the L1id field of the ROD header which should increase by one at every event. If possible the ROD should be programmed to send events at a sustained rate high enough to saturate the receiving end of the readout link, in order to validate the flow-control in this configuration. Alternatively, the receiver program[2] can be slowed down via a command line option. The activation of the XOFF can be checked by observing the flow-control indicator on the S-LINK cards.

d) Prepare a file containing the test-event which is being sent by the ROD.

e) Run the S-LINK test program[2] with format and data verification.

f) The format verification will check that the event header and trailer produced by the ROD follow the format outlined in Appendix C.

g) The data verification will check that the event data arrive correctly.

2.3 Test Results

For every test item listed in Section 2.1 a global PASS/FAIL result shall be given. In case that a test item foresees a number of steps, the outcome of every step described in the test procedure should be documented.

3 Summary

A set of tests has been listed to test the S-LINK interface of the ROD and the format of the data it sends. The successful completion of these tests with the compilation of the test report is a prerequisite to the integration of the ROD with the TDAQ system, and will assure a smooth integration between these systems.

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1. Several S-LINK interface cards can be used on the PC:

a) SSPCI [4]: 1st generation AMCC based 32-bit/33MHz PCI interface card. Only 5V LDC mezzanine cards can be used with this interface. It cannot sustain the full S-LINK bandwidth of 160MByte/s. Use the slink_dst program with this interface card.

b) S32PCI64 [5]: 64-bit/66MHz PCI interface card. Only 3.3V LDC mezzanine cards can be used with this interface. Requires a PC motherboard with a 3.3V PCI slot. <http://hsi.web.cern.ch/HSI/s-link/devices/s32pci64/slot-types.html>. The S32PCI64 card has to be programmed with the single-channel FILAR firmware[6] in order to work with the filar_slink_dst program.

c) FILAR [7]: 64-bit/66MHz PCI interface card with four integrated HOLA LDC channels. Also requires a PC motherboard with a 3.3V PCI slot.

2. There are one slink_dst and one filar_slink_dst test program as part of the DataFlow distribution software. Execute “(filar_)slink_dst -h” for further information. This program checks the correctness of the S-LINK status words and of the ROD header and trailer. It is also able to read a file provided by the ROD developer, which contains a ROD test event, and compares it with the incoming data.

4 References

[1]http://hsi.web.cern.ch/HSI/s-link/spec/

[2]C. Bee et al, The event format in the ATLAS DAQ/EF prototype -1, ATL-DAQ-98-129, http://doc.cern.ch//archive/electronic/cern/others/atlnot/Note/daq/daq-98-129.pdf

[3]ROD Working Group, ATLAS Readout Link Recommentdations of the Detector Interface Group, ATL-DAQ-2002-007, http://doc.cern.ch//archive/electronic/cern/others/atlnot/Note/daq/daq-2002-007.pdf

[4]SSPCI: Simple S-LINK to PCI interface. http://hsi.web.cern.ch/HSI/s-link/devices/slink-pci/

[5]S32PCI64: S-LINK to 64-bit/66MHz PCI interface. http://hsi.web.cern.ch/HSI/s-link/devices/s32pci64/

[6]Single-channel FILAR firmware for the S32PCI64 card. http://edms.cern.ch/document/348746/

[7]FILAR: Quad HOLA S-LINK to 64-bit/66MHz PCI interface. http://hsi.web.cern.ch/HSI/s-link/devices/filar/

[8]ATLAS DataFlow software distribution, http://atddoc.cern.ch/cmt/releases/df/

[9]http://hsi.web.cern.ch/HSI/s-link/products.html#Testing

[10]SLIDAD user manual,<http://hsi.web.cern.ch/HSI/s-link/devices/slidad/>

[11]HP16500B Logic state analyzer setup files, <http://edms.cern.ch/document/304072/2>

[12]ATLAS Read Out Drivers: Endianness, https://edms.cern.ch/document/390276/1

[13]ATLAS Read Out Drivers: specification for BCID and L1ID, document in preparation.

Appendix A: S-LINK Signals

In the following paragraphs the definition of the S-LINK signals which have to be taken into account by ROD designers is recalled, to clarify their meaning.

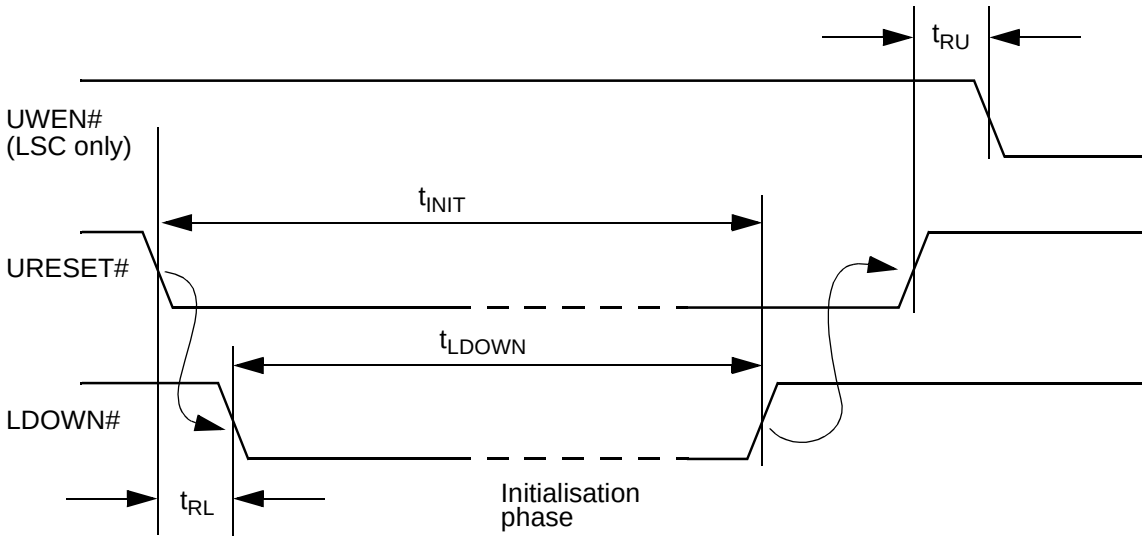
LDOWN# - Link Down

The LDOWN# signal shows that there is a serious, often fatal, problem with a link. For example the fibre connection is broken or the other side of the link is not powered. When LDOWN# is active, you should reset the link to see if you can go out of this state. Once the LDOWN# signal is inactive (the link is up), the link will function correctly for a long period of time (several days) and it will not need a reset until another fatal error occurs. The link will normally not go down on bit errors. Bit errors in the data will show up by the LDERR# line and in bits 0 and 1 in control words.

RESET# - Reset

Only when the LDOWN# line is active, a reset is needed. After power-up a link normally needs only once a reset and will function after that autonomously until a fatal error or power-down occurs. The RESET# signal should follow a defined handshake with the LDOWN# signal as shown in figure 1. The figure shows that you may only 'remove' the RESET# signal after the LDOWN# signal has gone up. So the RESET# signal may not be a simple pulse nor may it be removed while the LDOWN# signal is still low.

Figure 1: The S-LINK reset handshake



LFF# - Link Full Flag

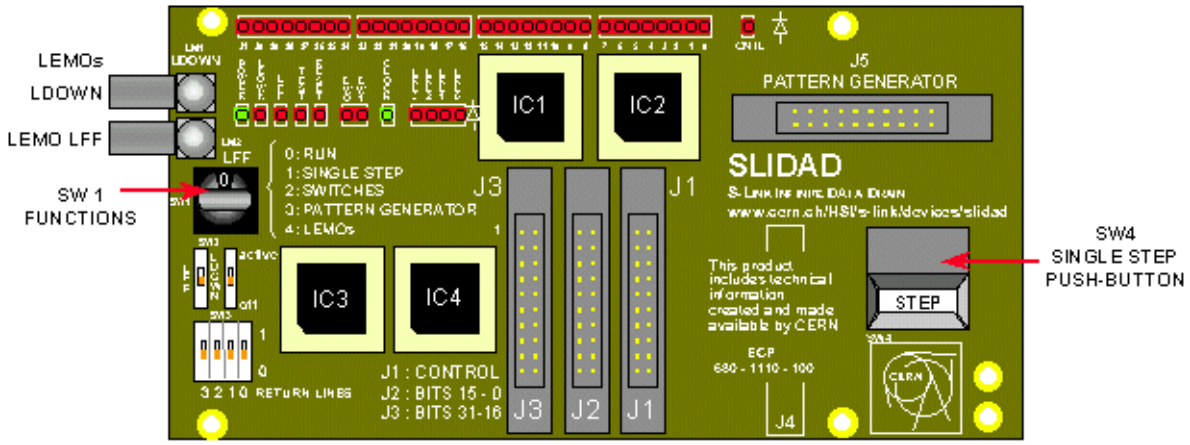
The Link Full Flag signals that the small buffer in the Link Source Card is almost full. This can be caused by the ROS who cannot accept more data or by the LSC itself if the ROD tries to send data faster than the physical link can handle. Once the LFF# signal gets asserted, the ROD may still send two words at maximum. If the ROD sends more than those two words, either data will get lost or even more serious effects may happen such as a link that freezes. Once LFF# deasserts again, the ROD may start sending new data.

Appendix B: S-link Testing Devices

A series of devices and adapters have been developed for ROD designers in order to allow the testing of their S-LINK interface without having to setup a real S-LINK with additional software at the receiving side. These devices are described in detail in [9]. The most relevant ones for ROD designers are the SLIDAD [10] and the SLIBOX devices.

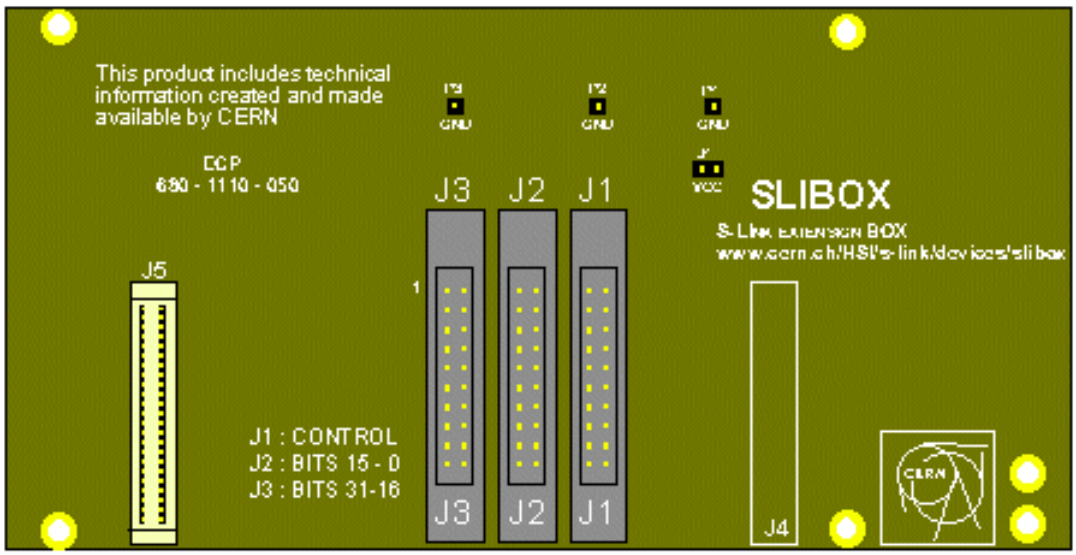
The SLIDAD is a standalone device that connects to the S-LINK connector of a ROD. It can be used to test the hardware of a ROD at its S-LINK interface without having to set up a real S-LINK with software on the receiving side. The SLIDAD is plugged in instead of an LSC on the ROD and shows the data that is sent by it. The data sent can be directly seen the on LED's and a logic state analyser may be connected to the three 20-pin connectors. The values of the return lines may also be set. With the single-step mode data can even be received and checked on a word-by-word basis. Advanced set-up and trigger files for HP16500 Logic State analysers [11] are available. Depending on the power supply used, a 3.3 Volt and a 5 Volt version exist.

Figure 2: The SLIDAD.



The SLIBOX is an S-LINK extender with three connectors that can connect to a Hewlett-Packard or to other Logic State Analyzers. It can be used to spy on all S-LINK signals in a working system and is connected between the ROD and the LSC.

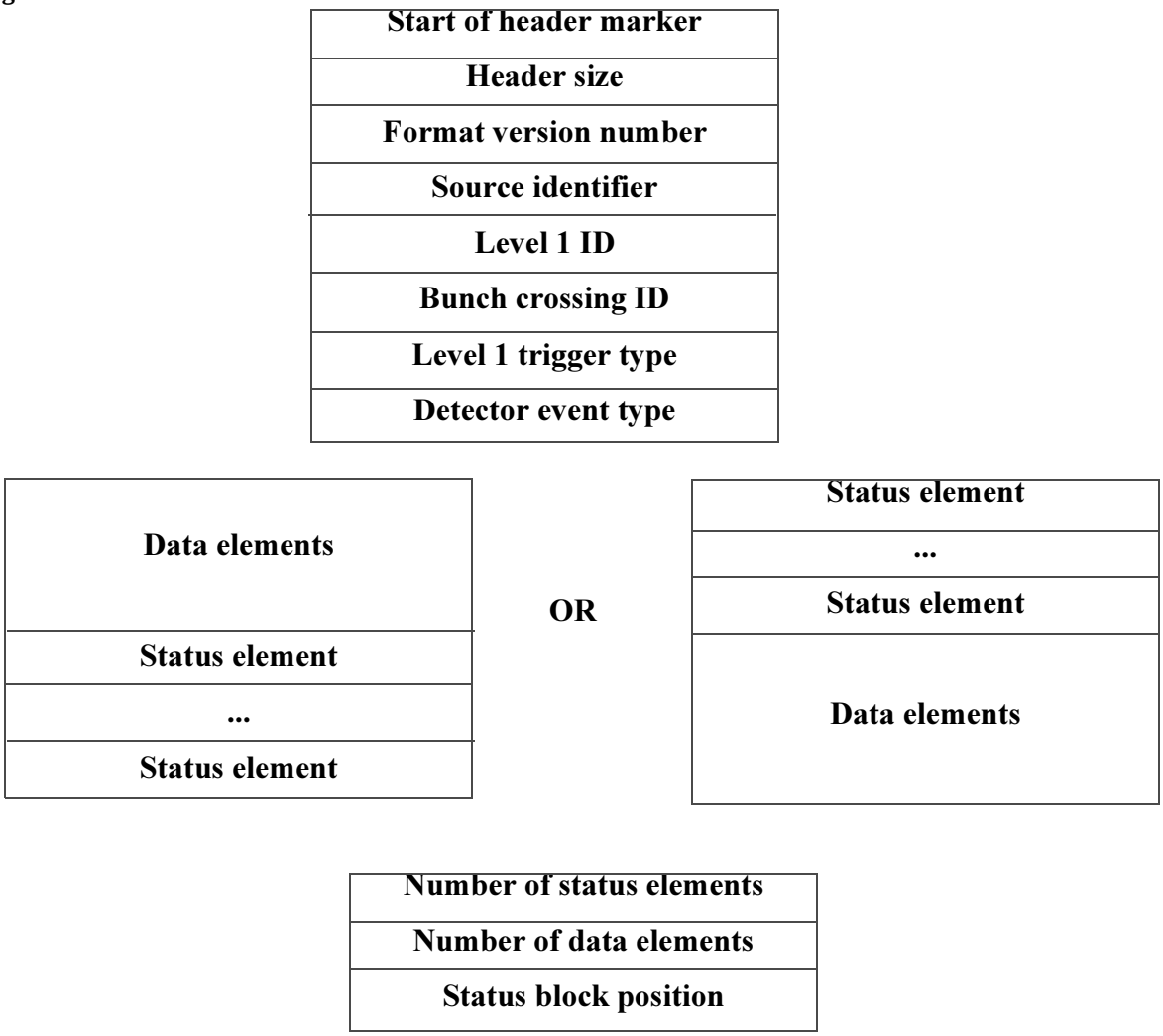
Figure 3: The SLIBOX



Appendix C: The ROD Event Format

The event format has been specified in [2]. Here we briefly recall the ROD data format, which is shown in figure 4. For the presentation of the fields, Big-endian byte ordering has been chosen. The byte order in the RODs has been specified in [12].

Figure 4: ROD data format.



For the ROD the fields (each a 32 bit integer) should be filled as follows:

Field	Description
Start of header marker	*0xee1234ee*
Header size	*8 (unit is 32 bit words)*
Format version number	*32 bit integer specifying the version of the ROD fragment format. At present 0x0202xxxx. The lower 16 bits are used by detectors to indicate their data format version.*
Source identifier	*see [2], section 5.2, page 11.*

Field	Description
Level 1 ID	*Extended L1ID formed by the 24-bit L1ID generated in the TTCrx and the 8-bit ECRID implemented in the ROD. The value of the first extended level 1 ID is specified in [13].*
Bunch crossing ID	*12-bit bunch crossing identifier generated in the TTCrx. The value of the first bunch crossing ID is specified in [13].*
Level 1 trigger type	*8-bit word generated by the Central Trigger Processor and transmitted by the TTC.*
Detector event type	*this element allows additional information to be supplied on the type of event, particularly in case of calibration events.*
Status element	*the first status element must indicate the global status of the fragment, a non-zero value indicating that the fragment is corrupted.*
Number of status elements	*(unit is 32 bit words!)*
Number of data elements	*(unit is 32 bit words!)*
Status block position	*0 indicates that the status block precedes the data block, 1 indicates that the status block follows the data block.*

With the S-LINK implementation of the ROL, the header and trailer the ROD fragment has to be framed with S-LINK control words. Each ROD fragment is preceded and terminated by a single S-LINK control word. These control words are referred to as the Beginning of Fragment and the End of Fragment. The words are 32 bits long and take the values

Beginning of Fragment	0xb0f0rrrr
End of Fragment	0xe0f0rrrr

The lowest 4 bits are used by S-LINK to report transmission errors and are therefore reserved. All 16 lower bits should be set to 0 prior to transmission of the control words.