ATLAS TileCal Read Out Driver production

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ABSTRACT: The production tests of the 38 ATLAS TileCal Read Out Drivers (RODs) are presented in this paper. The hardware specifications and firmware functionality of the RODs modules, the test-bench and the test procedure to qualify the boards are described. Finally the performance results, the temperature studies and high rate tests are shown and discussed.

KEYWORDS: Digital electronic circuits; Data acquisition circuits.
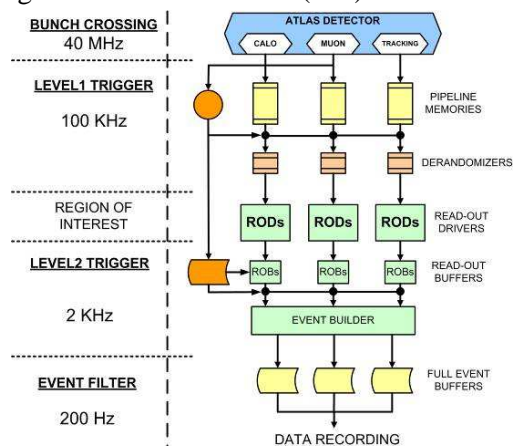
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Contents

1. Introduction

The ROD system of the ATLAS Hadronic Tile Calorimeter (TileCal) is placed between the first and the second level trigger and consists of four ROD crates (figure 1). Each ROD crate contains eight RODs and eight Transition Modules (TM) and reads out one out of four partitions

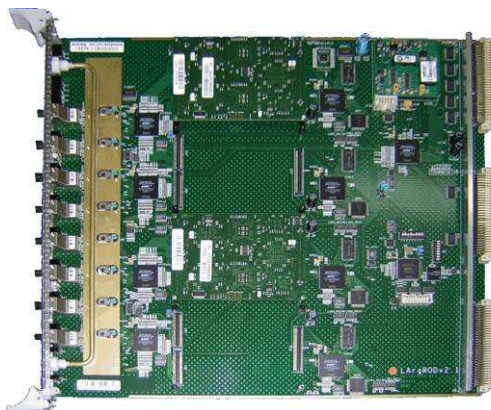**Figure 1.** ATLAS three level trigger architecture.

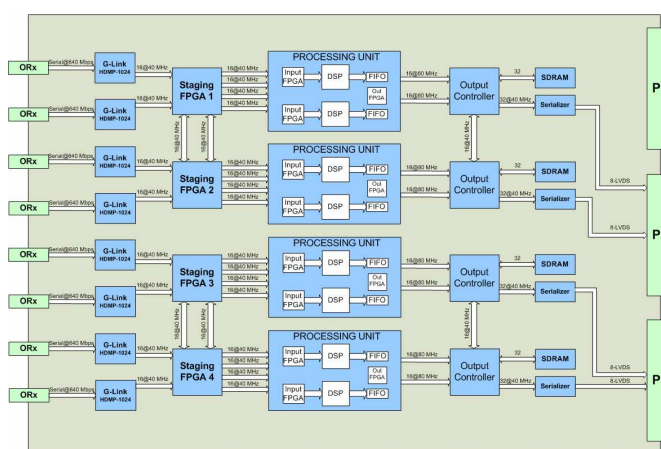**Figure 2.** ROD motherboard with 2 Processing Units.

Figure 3. Diagram of the ATLAS calorimeters common ROD.

in the calorimeter [1]. Therefore, 32 RODs and 32 TMs are needed in order to read out the whole calorimeter. Taking into account the spare units, we have produced and tested a total amount of 38 units of RODs and TMs.

1.1 The TileCal ROD module

Both the Liquid Argon (LAr) electromagnetic and the Tile hadronic calorimeters in ATLAS use a common ROD motherboard (figure 2) adapted to the specifications required in each case [1]. For this reason, the motherboards were produced together.

Figure 3 shows a diagram of the ATLAS calorimeters common ROD including the main components within the board [2].

Concerning the firmware, specific code for the TileCal ROD in the StagingFPGA, InputFPGA and DSPs is used [1]. As the InputFPGA and DSP code is downloaded at configuration time, only the StagingFPGA code has to be downloaded before the beginning of the tests. Besides, if some code is upgraded for specific or common firmware, it has to be checked and validated prior to be updated in all the boards.

Regarding the TMs [3], the difference between both calorimeters is the number of High-speed Optical Link for ATLAS (HOLA) mezzanine cards mounted on the boards. LAr ROD system implements four HOLAs per TM, whereas TileCal system uses two HOLAs per TM [1].
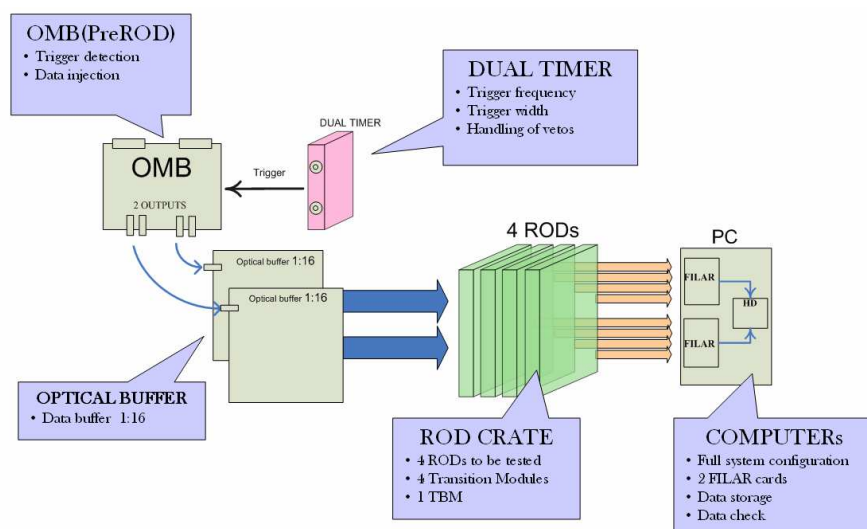
Figure 4. Test-bench diagram.

2. Test-bench description

The test-bench mounted in the lab at IFIC-Valencia for the TileCal RODs validation was divided into an injection part, a ROD crate and an acquisition system (figure 4).

The Front-End Board (FEB) was emulated by injecting data to the ROD with one Optical Multiplexer Board (OMB) 6U prototype, two Optical Buffers (OB) and a dual timer to control the rate of injection.

Up to four RODs in a crate could receive and process data simultaneously and a PC system equipped with 2 Input Links for Atlas Readout (FILAR) cards gathered, stored and checked all the data coming from the RODs.

Furthermore, one more computer was included in the setup as the main user interface computer responsible for the configuration tasks of all the devices in the test-bench chain.

### 2.1 Optical Multiplexer Board prototype

To reduce data loss due to radiation effect the TileCal collaboration decided to include data redundancy in the output links of the FEB by means of doubling the number of optical links per channel which would transmit the same data out of the detector. In this way if a single event upset occurs on data on one link, it is very probable that the other link be safe due to radiation space distribution properties inside the detector.

Unfortunately, ROD card has only one input connector for each front-end channel because in initial plans of using two links to transmit the data for redundancy was ruled out because of the incurred cost. For this reason and to take advantage of data redundancy and keep the original ROD design, an OMB also known as Pre-ROD was envisaged [4]. This board would be able to provide, in case of error in one link, the correct data to the ROD input by analyzing the Cyclic Redundancy Codes (CRC) of the data packets on both links coming from the FEB.

In the development of the work a new functionality for OMB was proposed. Because RODs should be tested in production stages and provided that in the first moments of LHC operation data may not always be available from front-end, it was suggested to include a "Data Injector Mode" to use the OMB like data pattern injector for ROD test and verification tasks.

Figure 5. Optical Multiplexer Board 6U prototype.
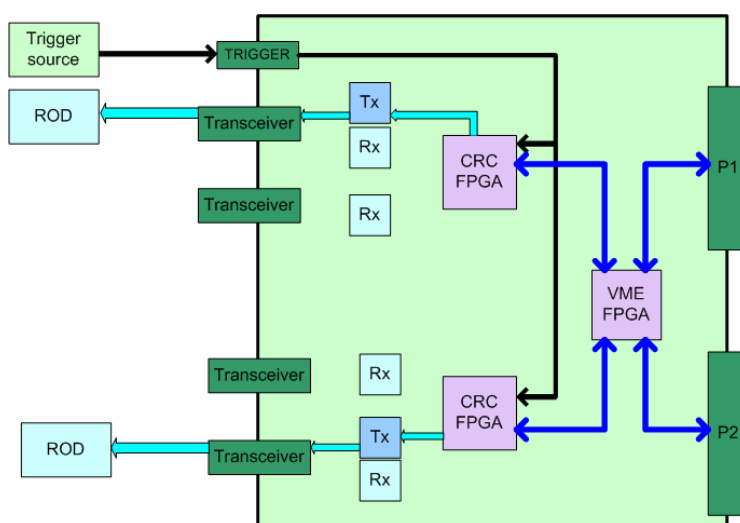
Figure 6. OMB injection mode data flow.

This function was used during the ROD production and the OMB 6U prototypes (figure 5) injected data to the RODs to verify their correct functionality. Figure 6 shows the data flow of the OMB 6U in the injection mode.

This injection mode contains two operation modes. One is the, so-called, counter mode where all the words inside an event are equal. The other one is the memory injection mode where it is possible to download any data file into the OMB and inject it. During the ROD production the counter mode was used to inject data towards RODs.

If the injection mode is selected the OMB has to receive a trigger signal in order to inject an event. There are two trigger modes. One is the external trigger NIM signal. The other is internally generated in the VME_FPGA. In both cases the maximum trigger frequency is determined by the time it takes to inject a full event. The OMB injects 16-bit words at 40 MHz. For instance, injecting an event with 200 words of 32 bits would take about 10 µs (100 kHz). However taking into account that data injection does not starts immediately after a trigger signal is received, it takes more than 10 µs for a 200 words event. The maximum injection rate for a 9 samples event (~180 words) measured experimentally is 93 kHz. Nevertheless during the high rate tests performed for the RODs at CERN, 7 samples events were used (~148 words) and more than 100 KHz was achieved. This type of events with 7 samples will be used in the

Figure 7. Optical Buffer 1:16.

ATLAS experiment in high rate runs. The external trigger mode was used to select the injection rate in the ROD production tests.

2.2 Optical Buffer 1:16

The OB is a 9U VME board specifically designed for ROD production (figure 7). As the OMB 6U prototype offers only two optical outputs and the ROD has 8 inputs, the OB was designed in order to increase the number of links injecting data to the RODs. The OB receives one optical input, converts the signal into LVPECL, and repeats it to 16 optical outputs with clock drivers.

With only one OMB 6U prototype and 2 OBs we had 32 links, which is enough to inject data to 4 RODs at the same time. It represents a half partition of the TileCal detector.

In counter mode, the OMB was programmed to inject different events through each output. The two outputs were repeated with two OBs. Note that to inject only two kinds of events to the ROD is not a problem as each DSP process the data coming from two inputs and is not correlated to others.

2.3 ROD and injection crates

Two crates were used during the ROD production. The first one was utilized as an injection crate, whereas the second one as a ROD crate. The crates used in the ROD production tasks were WIENER VME -64x Series 6000 LHC and the Single Board Computer selected as the VME ATLAS ROD Crate Controller (RCC) was the VP 110/01X from Concurrent Technologies. With these crates and RCCs we had VME access to every board inserted in the crates.

The injection crate was composed of a TTCvi for trigger configuration, an OMB 6U as data generator and the OB as a data repeater. In this case, the RCC was used for the configuration of the TTCvi and the OMB. In addition, a TTCex and a ROD Busy Module were used in order to test the RODs with the whole TileCal data acquisition system

The ROD crate contained the RODs to be tested, the TMs and the Trigger and Busy Module (TBM) to collect the busy signal from all the RODs in the crate and to make the veto to the trigger.

2.4 Computers and software

Three computers were used during the production for configuration tasks, acquisition and for data checking. The software utilized in the configuration of the tests was the ATLAS Trigger and Data Acquisition official software (TDAQ) adapted to our production tasks [6].

One of the computers was used to run the main partition of the TDAQ software. The TDAQ presents a graphical user interface and it was utilized for the configuration of the tests (figure 8). A set of user defined applications for the TDAQ handled the CRC error checking during the dynamic tests. The results were displayed in another DAQ panel were the number of
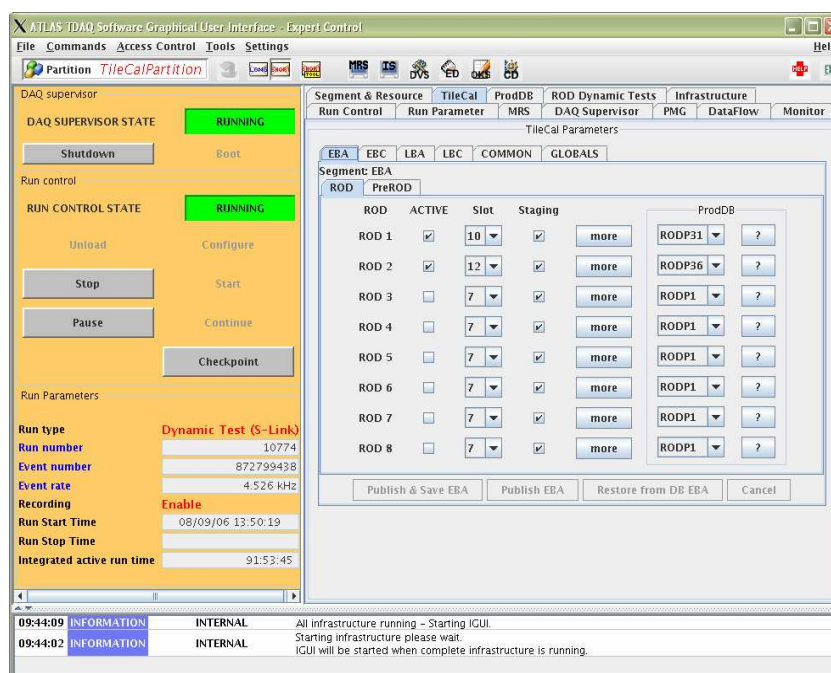
Figure 8. TDAQ software graphic user interface.

errors detected during a run was shown. Other information like run number, integrated time, number of events processed, etc., was shown in the same display. Besides, when a run was finished another user defined panel stored all this information in the ROD production database (see subsection 3.5).

Two more computers were used for data acquisition and data checking coming from the ROD system. The first one was a dual CPU with 2 Four FILAR cards installed. These 2 FILAR cards read out up to 4 RODs, and store the data in a shared file system. The second computer, with access to this shared file system, checked the data online.

3. Production tests

The ROD validation was divided into two different phases. In the first one, all the ATLAS calorimeters common RODs have been tested. These tests were made at the industry level and at the University of Geneva. Afterwards, the RODs were adapted to TileCal requirements and finally validated with this configuration.

3.1 Tests of the ATLAS calorimeters common RODs

The ATLAS calorimeters common ROD motherboards were made in TechCI (France), and the components assembly in Seisystem (Italy). The RODs were delivered from industry after some general tests and mechanical checks had been done. With the Processing Units (PU) already installed in the ROD motherboard, some JTAG boundary scan tests were made to the system. Nevertheless, the PUs were checked with X-ray tests previously to its insertion in the ROD motherboard. If all these tests were passed, the RODs were delivered to the UniGe, responsible of the validation of ATLAS calorimeters common RODs [5]. The UniGe group developed several functionality tests in order to check the correct dataflow across the boards. For this purpose, some static tests were made to prove the correct operation of programmable devices. Then, some data path tests proved the correct communication between the StagingFPGA and the

LEVEL	RODs	RATE	MINIMUM TIME
0	1	Three DVS tests	
1	1	200 Hz	4 h.
2	1	1 KHz	8 h.
3	4	1 KHz	72 h.

Table 1. Four level tests protocol.

Output Controller (OC) FPGA. Finally, dynamic tests with the ROD Injector as data generator, and the TMs for sending the data out, validated the whole ROD system. These dynamic tests were made at different frequencies of injection and operating in full and staging mode.

3.2 TileCal adaptation

Once the ATLAS calorimeters common RODs were validated at the UniGe, they were delivered to the TileCal group. Then, the first task was to adapt them to TileCal specifications, including hardware and firmware modifications in the boards [1]. The hardware modifications were made at the electronic laboratory at IFIC-Valencia and they included some changes of clocks and passive components in order to adapt the G-Link frequency of data reception. The number of PUs utilized in TileCal RODs was also adapted as only 2 PUs per ROD are used in TileCal (Staging mode), instead of the 4 used in the LAr subdetector (Full mode) [1].

Once the hardware modifications were done and with the boards already in the ROD crate, the firmware adaptation was realized. The specific firmware for TileCal was downloaded in the StagingFPGA, InputFPGA and in the DSP. Besides, the common firmware was updated as upgrades were available.

3.3 Validation tests of TileCal RODs

The ROD validation protocol consisted of a four-level test chain. Each ROD had to pass all the test levels in order to be validated. The first level, called level 0, was basically a static test composed of three Diagnostic and Verification System (DVS) tests. These DVS tests basically certified the correct access through VME to every register inside all the programmable devices on the ROD motherboard. Besides, the correct communication between the StagingFPGA and the OC FPGA was checked by sending several events from the internal memory of the StagingFPGA and reading them out with the OC FPGA. In order to consider the level 0 approved, each ROD had to pass at least three DVS tests.

Once a ROD has passed the level 0 tests, 3 levels of dynamic tests level 1, 2 and 3 are applied to the module. In these tests the OMB 6U board emulated the FE injecting data to the RODs. The data processed by RODs was stored and checked in the computers. The maximum trigger rate reached by the online check task was approximately 400 Hz. For higher rates, the software couldn't check all the events online, and only a percentage of the processed events were checked.

Level 1 test was a single ROD dynamic test at low rate. The trigger rate was 200 Hz and all the events passing across the ROD were checked. After more than 4 hours data processing without errors, the level 1 became approved. At that rate, no busy signals appear in the ROD system.

Level 2 test was also a single ROD dynamic test, but increasing the injection rate and number of hours of the run. In that case, the rate of the trigger was 1 KHz and only 40% of processed events were checked. Besides, some busy signals appeared caused by the storage of data coming from RODs. Thus, the correct busy handling was also checked in that test. The ROD had to process data without errors at least during one hour in order to pass the level 1 test.

Width	16 bit
Poly	1021 This is the divisor polynome
Init	FFFF This is the initial value of the register
Refin	CRC output is not reflected
Refout	CRC output checksum is reflected
Xorout	No XOR is performed to the CRC output
Check	ascii string "123456789" checksum is 29B1

Table 2. Specifications of the CRC utilized in the RODs production.
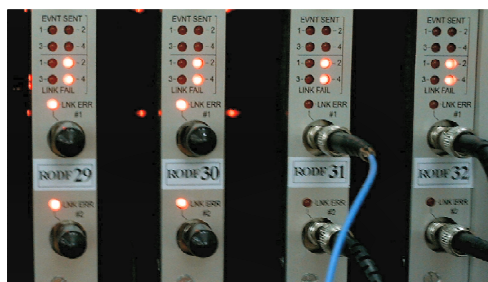
Figure 9. Final label in the ROD front panel.

Finally, the level 3 test was a multiple ROD burn-in test at high rate. In this case, four RODs were tested together during at least 72 hours. The trigger rate was selected to be 1 KHz, and only 10% of the processed events were checked.

If no errors were found during the 4 level tests, the ROD became validated and ready to be installed in the ATLAS electronics cavern (USA15) at CERN.

3.4 Data checking algorithms

The data processed by the RODs were checked online by two monitoring task algorithms. If the counter mode was selected in the OMB inside an event, all the words were equal and their value one unit higher than in the previous event. This check, allowed to verify the correct functioning of the ROD system.

In addition, as the OMB sent the CRC of each event attached as last word, it could be checked after the acquisition chain. The type of CRC utilized for data checking in ROD production was CRC-CCITT16. This type of CRC is also used in the TileCal experiment in order to check the correct data transmission between the front-end and the RODs. The full configuration of the CRC used is showed in table 2.

3.5 Production database

After their adaptation to TileCal requirements the RODs, PUs and TMs were labelled and introduced in a database. Each ROD motherboard had associated two PUs and one TM. The validation of a ROD implied the validation of the entire group, which is labelled with a final ROD (RODF) label. This label can be seen in the front panel of each validated ROD (figure 9). RODs are installed in the pit according to the component association introduced in the database.

The production database includes all the information about a ROD group. Besides, with the TDAQ software it was possible to save in the production database all the information related to each run. Thus, apart of the PUs and TM associated to each ROD and the firmware version of each programmable device inside a ROD, the production database includes all the tests done to every ROD.
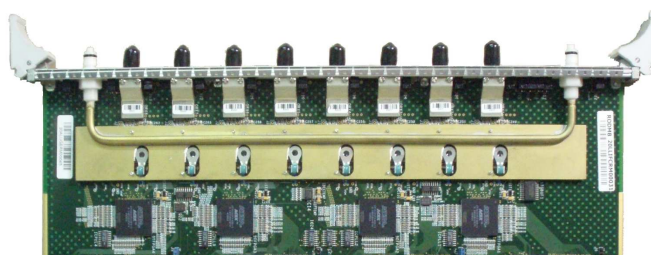
Figure 10. Water cooling circuit for the G-Links in the ATLAS calorimeters common ROD.

Finally, the incidents found during the production were also introduced in the production database. The production database is totally accessible from a web page.

4. Tests results

The number of ROD boards produced has been 38. For the read out of the experiment 32 boards are needed, and 6 units have been produced as spares. All the RODs produced have passed all the four level tests previously shown. It implies that each ROD has been processing data during at least 84 hours, has processed more than 264×10^6 events with at least 38×10^6 checked events without errors. Nevertheless, some extra runs were done during the production period in order to validate some firmware upgrades. All the runs were introduced in the production database and all they are counted as processing time by the RODs.

Considering all the tests done during the production period, the ROD system has been processing data during 3225 hours. A total of 13×10^9 events were processed during this time, and 1.7×10^9 events were checked without errors. The events injected by the OMB 6U and processed by the RODs during the production emulated an actual 9 samples event (176@32bits words). Thus, taking into account the number of bits processed by the ROD system, we obtain a bit error rate (BER) lower than 10^{-13}.

Nevertheless, as shown before the number of events processed by the ROD system during the production was approximately 1.7×10^9, which represents a run of 5 hours of the TileCal experiment at full expected rate (100 KHz).

4.1 Temperature tests

Apart from validating the correct functioning of each single ROD, we had to validate the cooling system selected for the TileCal ROD crates. The HDMP-1024 receiver, so-called G-Link, is used to build a high-speed data link for point-to-point communication. This chip receives a differential signal from the Optical Receivers (ORx), and parallelizes data coming from the front-end. In TileCal ROD, the G-Links are clocked at 40 MHz, leading to an input data rate of 640 Mbit/s (16 bits @ 40 MHz).The LAr G-Links are clocked at 80 MHz meaning a serial data rate of 1.28 Gbit/s. Rigorously it is beyond the manufacturer specifications. Nevertheless, the manufacturer guaranteed full functionality for selected chips as long as their case temperature is kept below 35ºC [7]. The standard air cooling system could not meet this requirement and a water cooling circuit was designed and mounted on the ROD motherboard over the G-Links chips, in order to guarantee a case temperature below 35ºC (figure 10).

For the TileCal requirements, the G-Link clocking at 40 MHz is well within the manufacturer specification, and it was decided not to use the water cooling system. In order to verify the correct functioning of the air cooling system some temperature studies were performed in the laboratory and in USA15 [8]. For these studies, the final configuration of ROD

G-Link Slot	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	45	45	49	49	55	55	49	45	45	46	49	62	55	55	45	45
2	45	45	55	55	55	55	47	45	45	49	49	66	62	55	45	45
3	45	45	55	55	55	55	45	45	45	49	47	62	62	55	45	45
4	45	45	49	49	49	55	45	44	45	49	47	62	55	49	45	45
5	42	44	47	49	47	49	45	43	45	46	45	55	55	47	44	45
6	40	43	45	45	45	46	43	40	43	45	45	55	49	45	43	43
7	36	40	45	45	43	45	40	36	40	45	43	45	45	45	40	40
8	32	36	36	40	36	36	32	32	36	40	36	43	40	36	36	36

Table 3. Temperature (in ºC) in all the G-Links in a 16 RODs partition in the lab.

G-Link Slot	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	40	36	36	36	36	36	40	36	36	45	44	44	47	45	45	40
2	43	37	44	36	40	40	43	40	40	45	45	45	49	45	45	45
3	43	36	44	36	36	40	43	40	36	45	45	45	49	45	45	43
4	40	36	43	36	36	40	40	36	36	45	44	43	46	45	45	40
5	36	36	40	36	36	36	40	36	36	43	43	40	45	45	44	36
6	36	35	36	36	32	36	36	32	32	40	40	36	45	45	40	36
7	32	32	36	32	29	32	32	29	29	36	36	35	40	42	36	32
8	28	28	28	28	28	28	28	28	28	29	29	28	32	36	30	29

Table 4. Temperature (in ºC) in all the G-Links in a 8 RODs partition in USA15.

modules per crate (8 RODs and 8 OMB 9U boards in a ROD crate) to be used at the pit was emulated. As the OMB 9U were not available, we emulated them in plugging 16 RODs in the same crate. With this setup the temperature was measured for all the G-Links in all the RODs after more than 48 hours of running. Table 3 shows these measurements for the lab tests.

Then, the test was repeated with the same setup in USA15. The temperature measurements after the same time of running are shown in table 4. Comparing table 3 and table 4 showed that the cooling system in USA15 worked better than in the lab and the temperature results showed lower values in all the cases.

In both cases, the warmest G-Links are the numbers 2 and 3 in all the RODs. It is due to the fact that the lower part of the ROD receive a major cold air flux from fans and that G-Link 1 in the upper part is also cooled by external air.

There is also a variation in the G-Link temperature with respect to the slot where the RODs are plugged. That's due to the implementation of the fans in the crate.

The temperature of all the G-Links after more than 48 hours of running was kept below 60ºC, which is well within the chip specifications (85ºC).

The StagingFPGA firmware was modified in order to set the temperature threshold for the alarm LED in the front panel of the ROD at 65ºC. At this temperature the ROD should work correctly but we considered that this temperature in any G-Link implies a wrong functioning in the cooling system.

4.2 High rate tests

During the TileCal commissioning phase at CERN, the final back-end acquisition chain composed of ROD modules and Read-Out Subsystems (ROS) was used. The ROS is the part of the ATLAS DataFlow system that accepts data from the detector RODs. This data are stored
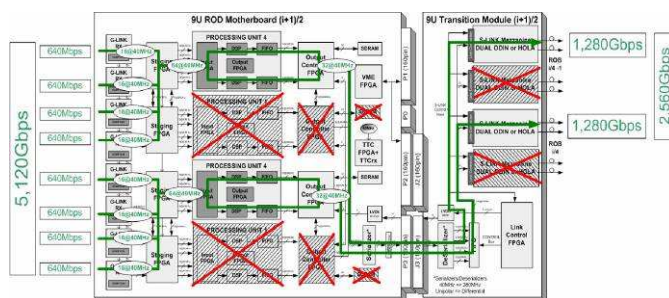
Figure 11. Input and output data bandwidth for the ROD system in the Staging mode.

Mode	High rate 7samples/1gain	Physics 9samples/1gain	Calibration 7samples/2gains
Full	100 KHz	100 KHz	76 KHz
Staging	69 KHz	57 KHz	38 KHz

Table 5. Theoretical limit rate for RODs as a function of the operation mode and the run type in copy mode.

Mode	High rate 7samples/1gain	Physics 9samples/1gain	Calibration 7samples/2gains
Full	100 KHz	100 KHz	75 KHz
Staging	65 KHz	55 KHz	35 KHz

Table 6. Limit rate experienced in tests as a function of the operation mode and the run type in copy mode.

and made available to the Level 2 Trigger and to the Event Builder (EB). A ROS machine is a PC that houses custom built buffers (ROBINs) and multi-port Gigabit Ethernet NICs. The processed data are sent to the ROBINs from the RODs through Read-Out Links (ROLs). Each ROBIN has 3 input channels and each ROS PC houses 4 ROBINs.

The setup mounted in our lab at CERN in order to test the ROD-ROS system at high rate was the same as used during the RODs validation but with ROBINs instead of FILAR cards. The ATLAS specifications require a maximum event rate of 100 KHz at the ROD level. This maximum rate can not be achieved by RODs in copy mode, due to the output data bandwidth when four FEBs are processed by one PU. Figure 11 shows the input and output data bandwidth for the ROD system in the Staging mode. In this case, the output data bandwidth is half of input data bandwidth.

Hence, if there is no data compression, the input event rate is limited to 50 KHz. In order to achieve the 100 KHz event rate it is needed to decrease the amount of data in the ROD output by disabling inputs or by sending only the reconstructed data instead of raw data.

These expected behaviours were observed during our tests at CERN. Firstly, we performed some tests in Staging mode (4 FEBs per PU) sending raw data and the expected 50 KHz limitation was observed.

Then, in order to achieve the maximum LHC rate, the ROD was configured in Full mode (2 FEBs per PU) and the injection event format was reduced to 7 samples and 1 gain which will be the format used in LHC for high rate runs. With this configuration the OMB-ROD-ROS chain was tested at 100 KHz.

5. Conclusions

The TileCal ROD production consisted in the fabrication of 38 ATLAS common RODs, their adaptation to TileCal requirements and their validation. The validation tests were performed with a complete ROD system composed of a ROD motherboard, two PUs and one TM. The test-bench designed for the ROD production continues being used on the DSP reconstruction routines tests since it is possible to emulate the front end with actual data.

The burn-in tests performed during the production period indicated a BER for the ROD system lower than 10^{-13}. It is better than the 10^{-12} BER specified given by the G-Link chip manufacturer.

The temperature tests performed on the ROD system proved that the air cooling system in USA15 works well and that there is no need for an extra water cooling.

The high rate tests performed at CERN corroborated the expected rate limitations at ROD level. Nevertheless, the maximum ATLAS event rate of 100 KHz has been achieved using event with 7 samples and 1 gain.

All these results are being corroborated during the TileCal commissioning, where the RODs are being integrated in the ATLAS data taking system. Real data from TileCal front end are being processed by the ROD system and successfully analyzed offline.

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