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TECHNICAL REPORT

Signal integrity studies at optical multiplexer board for TileCal system

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ABSTRACT: The Optical Multiplexer Board is a card included in the TileCal Data Acquisition System; it is designed to receive two optical fibers with same data from front-end boards and decided which has correct data.

Inside this card we have different transmission lines that need to be studied; signal integrity problems such as signal delay, reflection, distortion and coupling should be analyzed.

This paper presents the results of the signal integrity studies at the Optical Multiplexer Board for TileCal System.

KEYWORDS: Instrumentation for particle accelerators and storage rings - high energy (linear accelerators, synchrotrons); Hardware and accelerator control systems.

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Contents

1. Introduction	1
2. TileCal system	1
3. Signal integrity studies at OMB	3

1. Introduction

At the European Laboratory for Particle Physics (CERN) in Geneva, a new particle accelerator, the Large Hadron Collider (LHC) is presently being constructed. In the year 2008 beams of protons are expected to collide at center of mass energy of 14 TeV.

In parallel to the accelerator, two general purpose detectors, ATLAS and CMS, are being developed to investigate proton-proton collisions in the new energy domain and to study fundamental questions of particle physics.

This new generation of detectors requires highly hardened electronics, able to deal with a huge amount of data in real time. The work we present here is included in the studies and development currently carried out at the University of Valencia for the Optical Multiplexer Board of the hadronic calorimeter TileCal of ATLAS.

2. TileCal system

TileCal, the hadronic calorimeter of the ATLAS experiment, consists, in terms of electronic readout, of roughly 10000 channels read each 25 ns. Data gathered from these channels are digitized and transmitted to the Data Acquisition System (DAQ) [1] following a three level trigger system (figure 1).

Read Out Drivers (ROD) are placed between the first and second trigger levels. Their task is to pre-process and gather data coming from the Front End Boards (FEB) after a good first level trigger before sending them to the second level.

TileCal has a redundant data acquisition system; two optical fibers carry the same data from front-end electronics [2] to ROD. The reason for this is that radiation phenomena might cause malfunctions inside front-end electronics, as well as bit and burst errors over data ready to be transmitted to ROD card. The TileCal FrontEnd circuit which sends data to the ROD system is the Optical Interface Board (OIB). In this board two chips are of interest from the point of view of errors: a Field Programmable Gate Array (FPGA) and a Digital-to-Analog Converter (DAC), both sensitive to radiation and prone to fail [3]. The OIB was tested with proton beams in different areas and with different beam sizes and was found to fail in three different, non-destructive ways:

- Transient error in the data flow out to the ROD.
- Permanent errors in the data flow requiring FPGA reset.
- Latch-up error with an increment in current consumption of 60 mA.

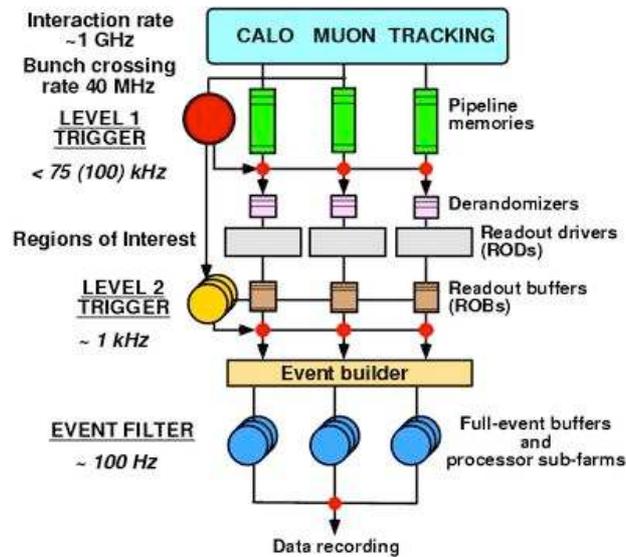


Figure 1. ATLAS three-level trigger architecture.

To reduce data loss due to radiation effect, the TileCal collaboration decided to include data redundancy in the output links of the OIB by means of doubling the number of optical fibers per channel which would transmit the same data out of the detector. In this way, should a radiation error occur on data on one fiber, it is very probable that the other fiber be safe due to radiation space distribution properties inside the detector.

Unfortunately, ROD card has only one input connector for each FrontEnd channel, because the original design responds to initial specifications which did not have considered radiation problems. For this reason and to take advantage of data redundancy and keep the original ROD design, a pre-ROD, also known as Optical Multiplexed Board (OMB), was envisaged. This board would be able to provide, in case of error, the correct data to the ROD input by analyzing the Cyclic Redundancy Codes (CRC) of the data packets on both fibers coming from the FEB.

The University of Valencia (Dept. of Electronic Engineering and dept. of Atomic Physics) and IFIC (Spain) team showed interest in this project and committed to make a first prototype to study technical viability. In particular, the main goals were:

- Data packet switching to take advantage of redundancy.
- Obtain real (production) costs.
- Have a development platform (HW - SW).
- Try different alternatives for data error analysis (CRC, etc.).

In the development of the work a new functionality for OMB was proposed. Because RODs should be tested in production stages and provided that in the first moments of LHC operation data may not always be available from FE, it was suggested to include a “Data Injector Mode”, to use the OMB like data pattern injector towards ROD for test and verification uses.

Figure 2 shows the final architecture for the acquisition chain of TileCal [4]. The OMB will be placed in ROD crates, each OMB will receive 16 fibers from the front end of the detector and will output 8 fibers to each ROD.

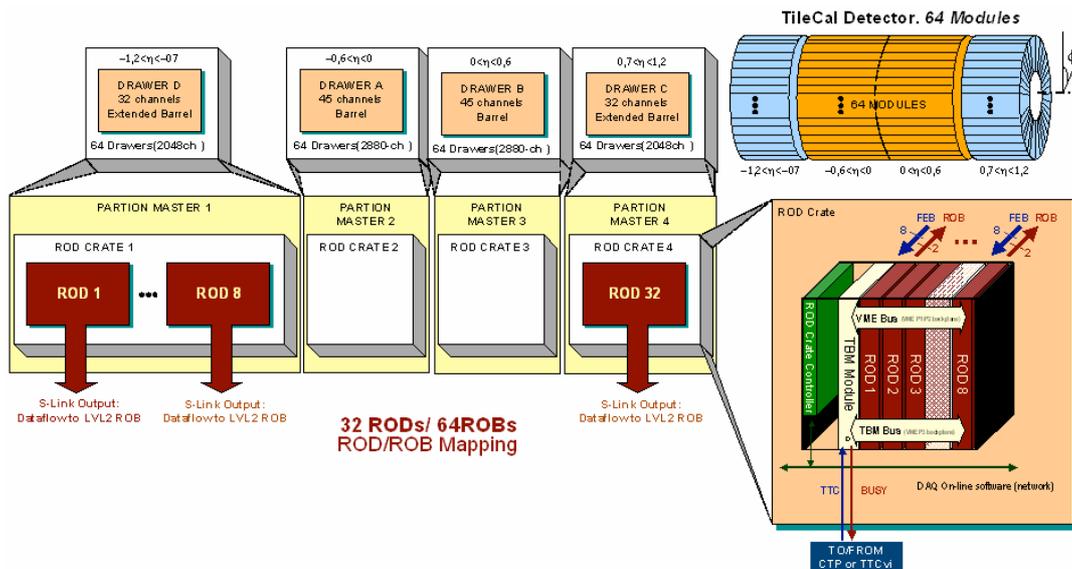


Figure 2. TileCal ROD general architecture organized around ROD crates.

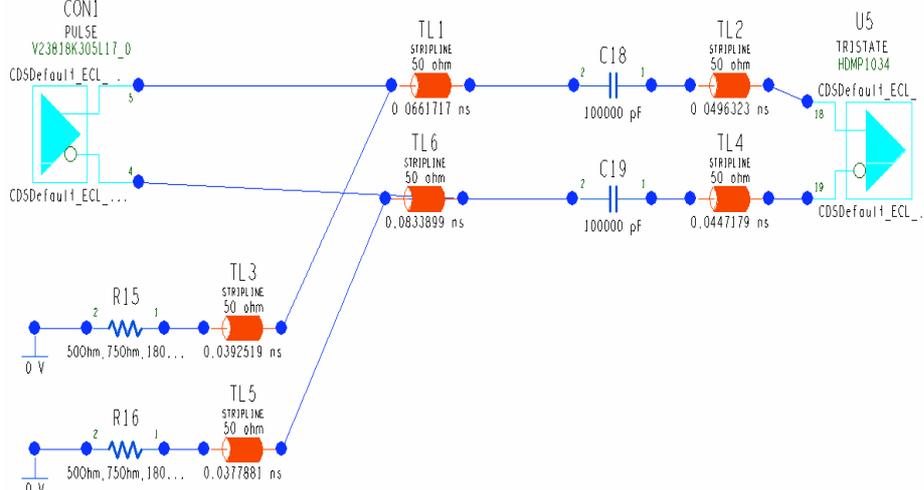


Figure 3. Differential lines topology from optical fiber connector to HDMP.

3. Signal integrity studies at OMB

One of the main aspects we cared about in the PCB design of the OMB was signal integrity. Even if the clock frequency used is not very high (40 MHz) it is true that we faced several 32-bit buses to be routed, so crosstalk might be something to worry about.

We carried signal integrity studies both in pre-layout and post-layout stages using Cadence SpectraQuest software [5]. Pre-layout analysis let us to establish the routing rules and the chose of termination resistors, if needed. Post-layout analysis verified the design taking into account the PCB layer stackup.

As an example, the differential lines connecting the Infineon fiberoptic transceivers and the HDMP chips at 640 Mbps were studied in a pre-layout phase. In this case we established the equal routing length and let the software simulate the behaviour with different termination resistors. Figure 3 shows the topology for this case.

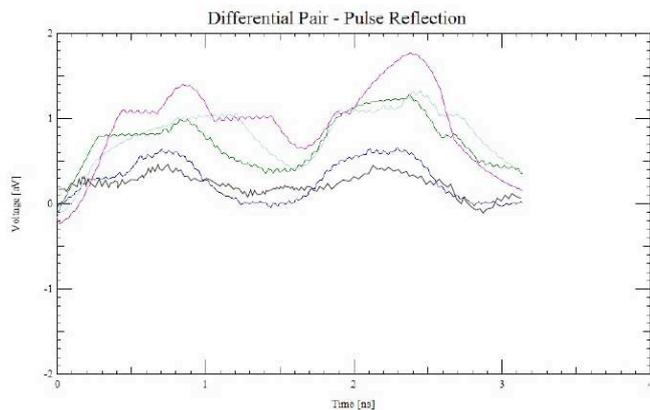


Figure 4. Received pulse at the HDMP input for different terminations.

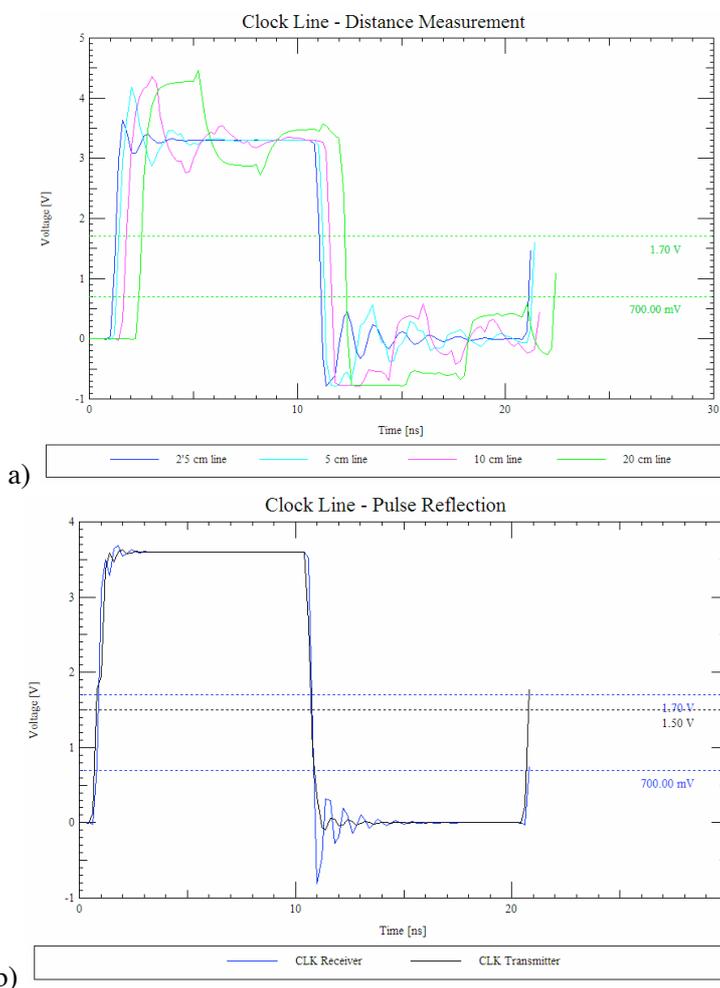


Figure 5. Clock line reflection simulations for (a) one and (b) multiple clocks.

The results of the simulation for different resistor values are shown in figure 4. From them a 180 ohm value has chosen as optimum termination.

Another important issue in high speed digital design is clock distribution. In our case we had the option to mount just one clock for all the HDMP's as we used one clock for each FPGA.



Figure 6. The optical multiplexer board prototype.

This option is very sensitive to trace distance and would imply strict routing rules which may lead (as we were very space limited) to an impossible solution. Besides, taking into account that input and output optical links need not to be synchronized between them, we preferred to use one clock device for each HDMP. Pre-layout simulations helped in this decision as the option with only one clock chip performed worse than the multiple clocks one. Figure 5 shows the simulations for one clock and multiple clocks. As it can be seen a multiple clock solution gives a better signal quality and so it was the solution adopted.

The OMB was built using a 12 layer PCB. The layer stackup was designed to minimize crosstalk between layers by routing the adjacent ones orthogonally. Each two internal layers are between power or ground planes for this same reason. Optical transceivers and serializers/deserializers chip signal are preferably routed on the top layer for faster signal transmission. Buses are routed in parallel with equal trace length for minimization of skew. Figure 6 shows a photograph of the OMB finally implemented.

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