
Optical Buffer 1:16

Internal Note

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Abstract

This document is a manual describing the functionality and the operation of the Optical Buffer 1:16 (OB). The OB was specially designed to repeat optical signals during the TileCal Read-Out drivers (ROD) production. The data generated in one Optical Multiplexer Board (OMB) 6U prototypes were repeated with two OB in order to inject data simultaneously to four RODs.



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1 Functionality

The Optical Buffer (OB) 1:16 was designed to repeat an optical data signal to 16 optical outputs. Figure 1 shows a picture of the OB with the front panel. The OB is a general optical fiber buffer and it can be used in multiple applications. Nevertheless it was developed to test the Read-out drivers (ROD) of the ATLAS Tile Calorimeter (TileCal) during the production of these boards at IFIC-Valencia. One optical data input is repeated to 16 optical fiber outputs with the same data signal. Since one ROD has 8 inputs [1] with four optical buffers and 4 optical fiber data signals it is possible to test one full TileCal partition crate with 8 RODs.

To divide an optical fiber data signal in a passive mode reduces the signal intensity. To avoid the intensity reduction of the signal the OB receives the optical signal and transforms it to an electrical LVPECL signal. This LVPECL signal is repeated to 16 LVPECL signals with a clock driver [2]. This clock driver is an active component and it is able to repeat the signal without losses. Finally these electrical signals are transmitted again to 16 optical fibers through optical transceivers[3].

Summary of functionalities:

- To receive one optical fiber data signal and transform it to a LVPECL electrical signal.
- Repeat this received signal to 16 optical fiber data signals.



Figure 1: Optical Buffer 1:16.

2 Specifications

The OB is a VME 9U standard card with the following technical specifications:

- Bus: VME bus standard, only used to take 3,3V power supply and grounding from the backplane connectors.
- Size: VME 9U standard (367 x 400 mm).

- Approximately power consumption $\sim 1,6A@3,3v$.
- Front-panel:
 - One RJ-45 style LC connector input.
 - 16 RJ-45 style LC connectors outputs.
 - One power LED.
- Multimode 850 nm and 1.0625 GBd Fibre Channel.
- Complies with Fibre Channel and Gigabit Ethernet.
- For distances for up to 700 m.
- Prepared for hold up to three bars to increase the PCB stability.

3 Circuit and schematics

The OB circuit consist in three VME connectors wherefrom are obtained the 3,3 volts needed and the grounding (Figure 1). Some pins in row a and b on J1 connector are interconnected in order to not disturb with other modules inserted in the crate.

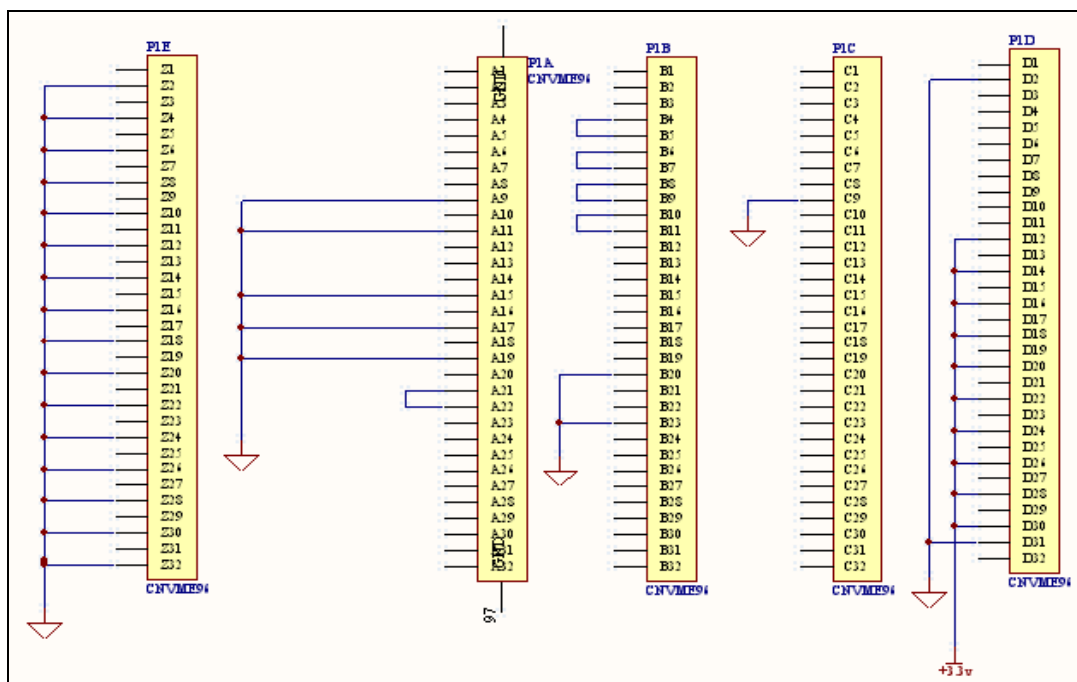


Figure 2: 5 pin rows of J1 VME connector for power supply and grounding.

The OB includes 16 Infineon® optical transceivers [3]. One is used to receive and transform an optical data signal into a LVPECL (Figure 2). This transceiver and the others 15 are used to transform and transmit this electrical signal into 16 optical outputs (Figure 3).

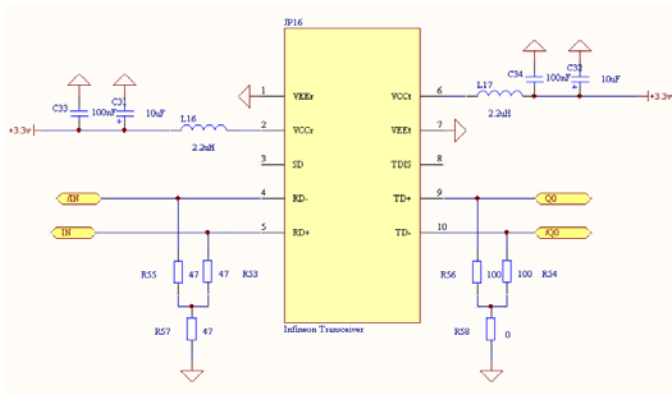


Figure 3: Optical transceiver emitter and receiver .

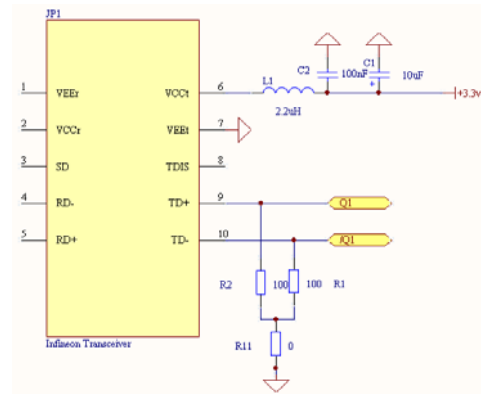


Figure 4: Optical transceiver emitter.

Besides 4 Freescale® clock drivers are mounted in the OB which are able to repeat one LVPECL signal to 10 outputs with a frequency of up to 2,7 GHz. We have used only 5 outputs of each clock driver to reduce the tracks length in order to avoid signal integrity problems (Figure 4).

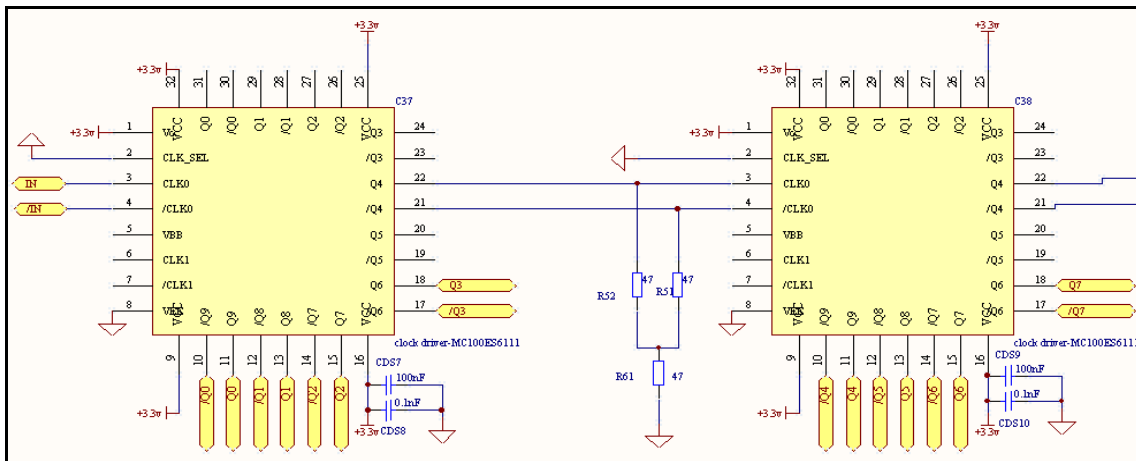


Figure 5: Clock drivers (MC100ES6111) connections.

Finally, a LED in the front-panel indicates that the board is powered with the needed 3,3 volts. The power lines are decoupled following the manufacturer specifications with capacitors to ground in the clock drivers and capacitors to ground and serial inductors in the transceiver chips.

The data signals are transmitted at 640 Mbps. In order to avoid signal integrity problems the data tracks have been terminated with resistors connected to ground. As the Optical transceiver includes an internal 100 Ohm resistor, each differential signal track has been matched with a 100 Ohm resistor connected to ground. The clock drivers input tracks have a ‘I’ termination connected to ground with three 47 Ohm resistors (figure 5)[1]. Besides, these termination resistors are placed close to the receiver component.

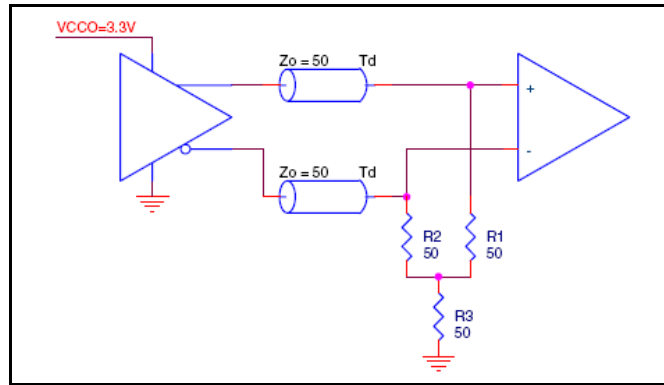


Figure 6: Equivalent 3.3v LVPECL termination implemented in clock drivers inputs.

4 Printed Circuit Board

The PCB is a two layer board with a 9U VME standard size. Data tracks are routed in the bottom layer whereas the top layer is used for power lines. To avoid crosstalk and other signal integrity problems one plane on each layer is connected to ground.

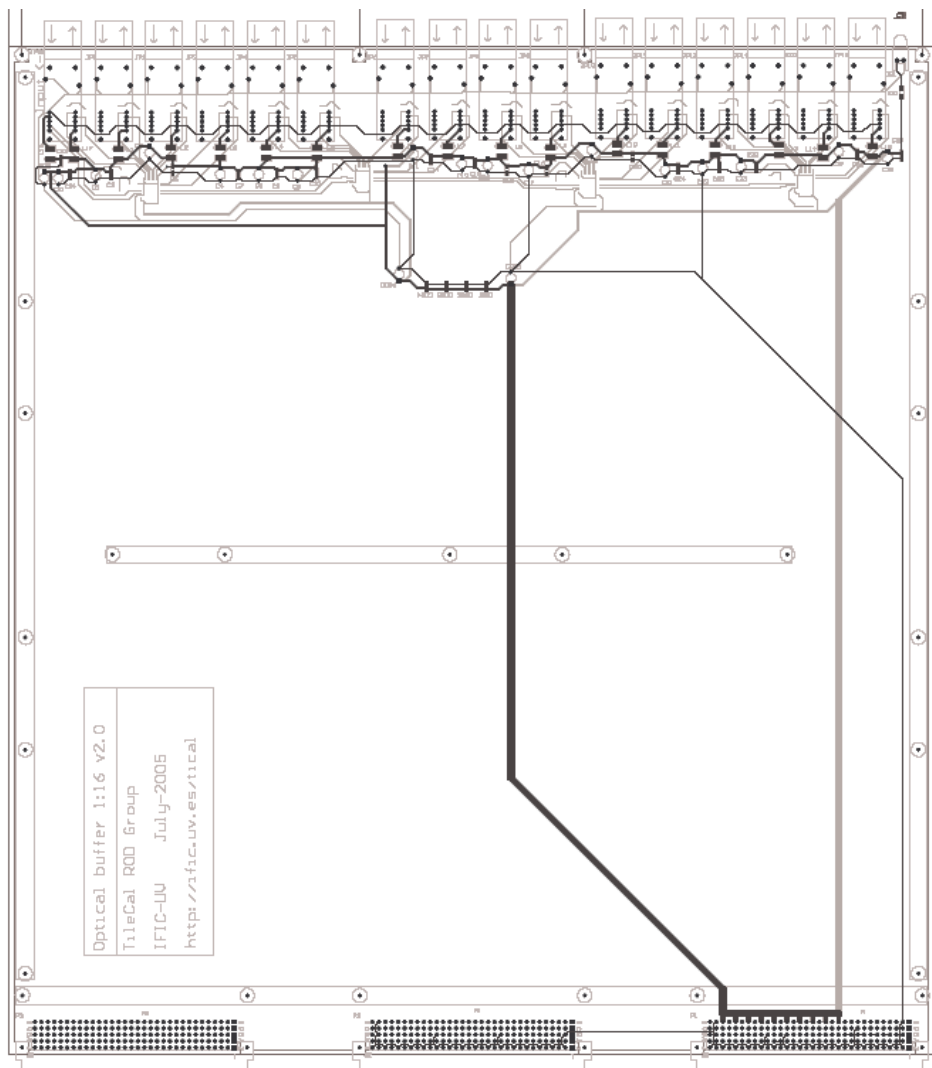


Figure 7: Optical buffer PCB design without ground planes.

4.1 Optical buffer PCB artwork

Figure 6 shows the whole sight of the PCB design without ground planes. All the components are placed in the top part of the board near the front panel to reduce the length of data tracks. Only the 3.3 volts tracks and the ground plane arrive to the VME connector placed in the bottom part of the PCB. The optical transceivers are placed just in the front panel whereas the clock drivers are distributed close to these connectors. In the bottom part are mounted the three VME connectors. Two tracks cross the PCB to provide the 3.3 V. needed by the clock drivers and the optical transceivers. These 3.3 V. tracks were routed with a controlled wide in order to fix a bug of the first OB prototype. The resistance of a PCB track is given by:

$$R = \rho \frac{L}{A}$$

where:

ρ is the resistivity of the track material in Ωm .

L is the track length in metres.

A is the track cross sectional area in square metres.

Then, a large track with a little cross section would present a high resistance. In the first OB prototype it was experienced a wrong power supply in the optical transceivers. To fix this problem it was increased the track width and it was routed two power supply tracks from the VME connectors to the components (Figure 6).

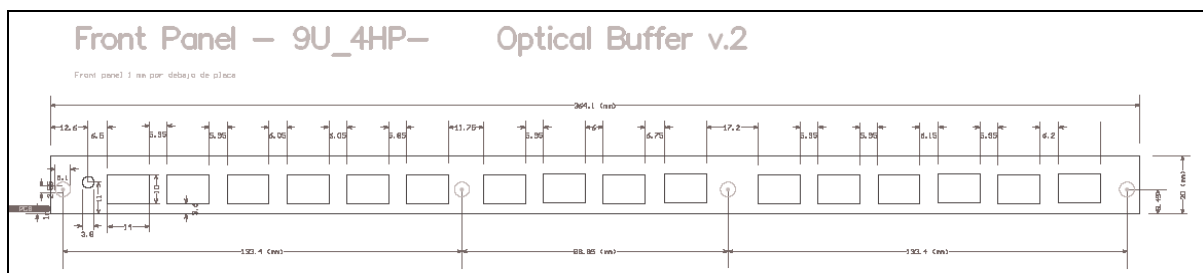


Figure 8: Optical buffer front panel – 9U, 4HP standard size.

5 Bill of materials

Description	Footprint	Value	Quantity
Surface Mount Capacitor	NSO805	100nF	25
Surface Mount Capacitor	NSO805	0.1nF	4
Polarized Capacitor	CAPR5-4x5	10uF	17
Polarized Capacitor	CAPR5-4x5	47uF	1
Polarized Capacitor	CAPR5-4x5	220uF	1
Clock driver- Freescale –MC100ES6111	32lead LQFP		4
LED	LED-0		1
Optical transceiver –Infineon-V23818-K305-L17	2x5		16
Inductor	NSO1812	3.3uH	17
VME connector	160 pins		3
Surface Mount Resistor	NSO1206	47	12
Surface Mount Resistor	NSO1206	200	1
Surface Mount Resistor	NSO1206	100	32
Surface Mount Resistor	NSO1206	0	16

Table 1: Bill of materials for Optical Buffer

6 TileCal ROD production

The OBs were used during the TileCal RODs production at IFIC (Valencia). The Optical Multiplexer Board (OMB) 6U was used as data generator to inject data to RODs, emulating the detector front end [4]. As the OMB 6U prototype offers only two optical outputs and the ROD has 8 inputs, the OB was designed in order to increase the number of links injecting data to the RODs. With only one OMB 6U prototype and 2 OBs we had 32 links, which is enough to inject data to 4 RODs at the same time (Figure 9). It represents a half partition of the TileCal detector.

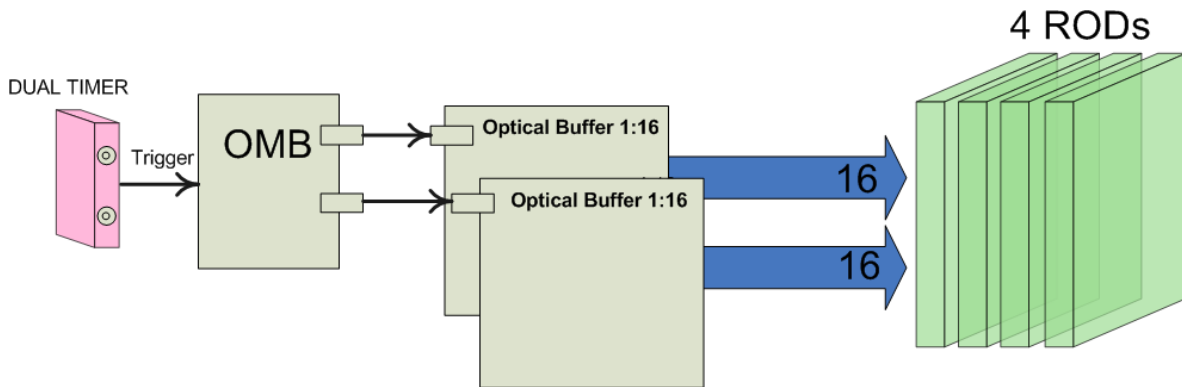


Figure 9: Data injection circuit in the ROD production test bench.

The OMB was programmed to inject different events through each output. The two outputs were repeated with two OBs. Note that to inject only two kinds of events to the ROD is not a problem as each DSP process the data coming from two inputs and each DSP works uncorrelated from others [1].

7 Conclusions

Considering all the tests done during the production period, the ROD system including the data injection components has been processing data during 3225 hours. A total of 13×10^9 events were processed during this time, and $1,7 \times 10^9$ events were checked without errors. The events injected by the OMB 6U, repeated by the OB and processed by the RODs during the production emulated an actual 9 samples event (176@32bits words). Thus, taking into account the number of bits processed by the ROD system, we obtain a bit error rate (BER) better than 10^{-13} .

8 References

- [1] J.Castelo et *al.*, “TileCal ROD Hardware and Software requirements,” ATLAS Internal Note ATL-TILECAL-2005-003, Feb. 2005
- [2] Freescale semiconductor, MC100ES6111, Technical data, Low Voltage 2.5/3.3 V Differential ECL/PECL/HSTL Fanout Buffer.
- [3] Infineon Technologies AG, V23818-K305-L18 Datasheet, Gigabit Ethernet Transceiver, <http://www.datasheetarchive.com/datasheet/pdf/68/687493.html>, 2001.
- [4] A. Valero et *al.* , “ Optical Multiplexer Board 6U Prototype”, ATLAS Internal Note. To be published.