TileCal ROD HW Specific Requirements to Use the New LArg Motherboard

A Report Document

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DRAFT

V1.0 previous to 5/6/2002 phone meeting

V1.1 Comments added since previous meeting

V1.2 New modifications proposed for new ROD motherboard PCB v2.0 (January 2004)

Abstract

This note represents a summary of the document "TileCal ROD HW Requirements and LArg compatibility" [3] and a meeting between the TiCal community and LArg representatives. Here we try to summarize the preferred hardware schemes discussed in [3], provide more details about specific compatibility needs and estimate a realistic time schedule for the hardware implementation of the TiCal needs in the LArg ROD motherboard.

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1 Preferred Hardware Architecture

1.1 Motivation of this selection

After the discussions at CERN the preferred solution is 2.3 in document [3] (Option 2: Using exactly the same PCB as LArg but clock select).

The schema is shown in Figure 1.

We consider this the better option as it maintains the compatibility between the calorimeters RODs. Using the same design will report:

- ✓ **Price**. Ordering higher quantities of boards and components reports lower prices.
- ✓ **Maintainability**. Using the same design gives a reliable product for solving future common problems in the installation and maintenance.
- ✓ **Number of RODs**. TiCal reduces the number of RODs from 64 to 32, thus hardly decreasing the project total cost.
- ✓ **Upgradeable solution**. With 32 RODs only one fiber is read-out per drawer, which is the TDR specification. Nevertheless, the Interface Links front-end boards are produced and designed with double optical transmitter in order to decrease by a factor of $\sqrt{2}$ the probability of errors in sending the same data fragment. So, if in a future high luminosity environment radiation problems with the links arise, more RODs could be added to readout all the double fibers (32 more RODs) or increase the number of more sensible and/or important channels to readout.

Only some changes at the input stage of the board are proposed (see Section 1.3). The rest of the board is maintained as the original LArg design except for using two Processing Units and two Output Controllers plus SDRAM data storage (see Section 1.2)

If we use the same hardware, only flexible software changes must be done specifically for TiCal. The parts which need to be programmed specifically for TiCal are the *staging FPGA*, the *Processing Unit (input FPGA, and DSP)*, and some adaptation in the VME libraries. The *Staging FPGA* must be able to manage the TiCal input data and control words and send them to the PU. The input FPGA of the PU must reorganize the TiCal data mapping and send it to the DSP to run custom optimal filtering algorithms implemented for the number of samples, bits/sample and output dataformat [2] of the TiCal detector. In principle the *Output Controller*, *TTC* and *VME* FPGA programs could be used as they are.

1.2 Hardware dataflow yield

We will show here how the use of two Processing Units and two Output Controllers plus SDRAM data storage are enough for the TiCal dataflow needs as shown in Figure 1. The LArg needs more processing power per link because this system processes 128 channels/link, while the TiCal system sends the links less saturated, and is not possible to send more than 48 channels/link due to drawer mechanical constraints. The real number of channels/link is 45 for the CB and 32 for the EB. These are the numbers:

- ✓ **Input bandwidth**. The maximum input BW of each link for a tilecal physic event is **467,2 Mbit/sec**[2]**,** and for four drawers is **1,825 Gbits/sec.** Taking into account that the input bandwidth of the Processing Unit is **2,5 Gbits/sec** (64bits@40Mhz) the input stage BW is solved.

- ✓ **The processing unit**. We need to process 154 channels (four drawers) in two **TMS320C6414@600MHz** DSPs, and each one of these units could perform **4800 MIPS**. This DSP has the same core with some improvements in number of registers and an enhanced DMA unit over the actual DSP we have tested, which is the **TMS320C6202@250MHz** with up to **2000 MIPS** [15]. With this unit we could process **45 channels** in around **5,5** m**s** if programmed in assembler and **15,5** m**s** if programmed in C code [4]. Therefore we conclude that we could, potentially, process 154 channels with the new PU **TMS320C6414@600MHz** [16] with **9600MIPs** (two DSPs) in **3,92** m**s** with assembler programming and around **11** m**s** with C language. As our limit is **10** m**s** at LVL1 100 KHz rate, if we assume improvements in the C compiler from Texas Instruments, one **could program the final system in a better maintainable C code** and **with only 2 Processing Unit mezzanines** installed in the motherboard.

- ✓ **Output Bandwidth**. The typical BW for 154 channels (four drawers) is **656 Mbits/sec** [2]. Then, an Output Controller FPGA of **1,28 Gbits/sec** (32@40MHz) has enough BW for the output of each Processing Unit (154 channels each). Two Output controllers with two mezzanine links mounted in the transition module will be enough for this configuration.

1.3 Details of the changes needed to the LArg board design

Only minor changes are needed to make the LArg design compatible with the TiCal readout system. They are summarized below:

- ✓ **From the Interface Links we need** to disable the *enhanced simplex mode* (pin ESMPXENB=0) in the HDMP1032. This is possible because this pin is controlled by an APEX FPGA (see reference [6]).

- ✓ **From the new LArg motherboard design we need**:

  - ➢ To **connect the CAV** line of the HDMP1024 to the Staging FPGA in order to receive control words (not only data words). In Figure 2 this line is highlighted in RED color.

- To **connect the FLAGSEL** line of HFMP1024 to Staging FPGA. LArg used the FLAG bit to mark the even and odd 16 bit fragments, and Tilecal use CAV (control bit) to mark the start of transmission and count for the even and odd 16 bit fragment. Tiles use the FLAG bit to mark the global CRC word so we need FLAGSEL set high, and LArg set low, so is needed to connect this pin to Staging FPGA for maintaining compatibility. In Figure 2 this line is highlighted in RED color.

- The connection of **FDIS**, **ACTIVE**, **LOOPEN** and **STAT1**, seems to be correct since they are standard as seen in *Figure 17 (page 33)* of the HDMP1024 datasheet [10]. The configuration is "*Simplex method III*".

- To **replace the LArg 80 MHz clock with the TiCal 40 MHz clock**. This is possible as the manufacturer has the two models that are pinout compatibles. This will allow to get the right reference clock for the G-link receivers. See Figure 3.

- In Section 2.1 of this document it is described the *TTC addressing scheme* of the TiCal subsystem. Because of this situation, we need flexibility **for setting the right address in the LArg board TTCrx chip**. If the chip is configured with an EEPROM it should be no problem for the ID, but if the configuration is hard-wired we prefer the ID address pins to be controlled by the FPGA.

- To **connect DIV1** and **DIV0** lines of the HDMP1024 chip to a CPLD in order to select the parallel word rate in range [**22,7-46,3**] MHz (DIV1=0, DIV0=1). LAr needs the parallel word rate in range [**43-75**] MHz (DIV1=0, DIV0=0) which has been tested in the first motherboard prototype and the deserializer was unable to lock the clock from the incoming data. For the right G-link clock lock we need a 40.00 MHz clock of 50 ppm as the one mounted in the Interface Card [6] but with different phase. It is better thus to mount the clock locally in the motherboard.

- The motherboard should be able to select between **3 clock sources** for the **G-link reference clock**:

  - **Clock oscillator of 40 MHz (50 ppm)** soldered in the motherboard

  - To be able to use the **general 40 MHz clock** in the motherboard selected with **0 ohm resistors**. This clock could come from:

    - **Local motherboard clock** : 40.00 MHz (local clock for working in absence of the TTC clock)

    - **TTC clock (from TTCrx)** : 40.08 MHz (LHC clock, it will not work since the Interface Card [6] serializer HDMP1032 uses a local 40 MHz quartz crystal for sending data).

- See "4 APPENDIX A" for specific details.

✓ **What needs to be tested**:

- We assume that the HDMP1032 TX of our Interface Links (not using the enhanced mode) is compatible with the HDMP1024 G-link RX chip. This is correct according

to the datasheet information of the manufacturer (Agilent). But some test must be done with prototype boards.

- The optical transceiver of the TiCal Interface Link is compatible with the optical receiver of the LArg boards as before, but this must be tested too.

- LArg has to build a complicated cooling system for the HDMP1024 chips clocked with 80 MHz. The chip power consumption should decrease with a lower switching frequency and thus one should check whether heat dissipation is required in terms of water cooling or assume common heat sinks are enough.

  - Two options are under investigation by the LArg. One is to modify the fan tray adding turbines which send air flow in a tube located on the motherboard with the G-link chip inside this tube. The other one is water cooling.

  - The power dissipation of a semiconductor is proportional to the frequency:

$$P_T = P_O + (P_S \cdot t_S + P_C \cdot 2t + P_{CON} \cdot t_{CON}) \cdot f \cdot N$$

where :

f = frequency

N = number of outputs at which bus contention occurs

P_{con} = power dissipation during bus contention

P_C = power dissipation when discharging the bus capacitance

P_O = quiescent power dissipation

P_S = power dissipation resulting from current spikes when output switches

t_{con} = duration of bus contention

t_S = duration of current spike

t = signal propagation time on the bus

By using a 40 MHz clock and a correct layout, this complicated and expensive cooling system might not be needed. As an experience example of this chip working at such frequency, G-Links LDCs have been built at CERN and proved to work at 40 MHz without cooling. Ideas for a robust layout can be found at http://hsi.web.cern.ch/HSI/s-link/devices/g-ldc/layout.html

- A CRC check of the input data must also be implemented. In principle it is preferred that the staging FPGA only routes data (*Altera ACEX 1k50 484 FineLineBGA)*, and data rearrangement and check done inside the input FPGA of the PU (probably two more powerful *Altera APEX 20k*). Since the CRC check takes several cells inside the FPGA, some simulations must be done in order to test if the program could be synthesized inside of one of these FPGAs.

- For these tests it is proposed to make a test board as described in "APPENDIX B: A Prototype Board for Testing the Input Stage of the LArg Design"

2 Preferred TTC Schema

It is assumed the preferred number of partitions for the TiCal read out to be 4 and organized around ϕ [0, 2π]. This means one partition for the left EB, one for the left CB, one for the the right CB and another one for the right EB. Figure 5 shows this configuration with 4 read out barrel partitions. The schema shown assumes 4 crates, but it could probably be implemented in 2 crates. This would allow to work with only central barrels in case not enough RODs would be available in an initial start of the run.

2.1 TTC Addressing

Each TTCrx chip on a partition is addressed from a TTCvi and must have a unique 14 bit address. This address is the only way to send messages to an individual chip and so to a ROD module (see references [1] and [22]).

In the Tical it is forseen to use the TTC system in:

- ✓ The 3-in-1 motherboards: 1 TTCrx chip per superdrawer.
- ✓ The digitizer system: 8 TTCrx chips per superdrawer.
- ✓ The RODs: 1 TTCrx chip per module

The TTCrx addressing scheme for the above devices is described below:

- ✓ Digitizers: 01 xxxx xxxx xxxx (where **x** is either **0** or **1** but not both zero)
- ✓ 3-in-1: 11 xxxx xxxx xxxx
- ✓ RODs: 10 xxxx xxxx xxxx
- ✓ Others: 00 xxxx xxxx xxxx

Each unique 14-bit channel identification (ID) number is read after reset, either from a serial PROM or by using the hard-wired ID mechanism from the ID<15:0> bus (see Chapter 8 of the TTCrx manual [23]). The TiCal would prefer these pull-up pins to be controlled by a PLD or through switches to allow a flexible selection of the configuration.

3 Cost of the Preferred Solution

An initial approximation to the project cost (using new LArg ROD boards with only 2 processing units and two output mezzanine links) is represented in Table 1[1].

Description	No.	Price/unit (CHF)	Total price (CHF)
9U VME ROD motherboard	32	4000	128000
Processing Units mezzanines	64	1500	96000
9U VME Transition Module with output links	32	2500	80000
S-Link HOLA 2.5Gbps LSC mezzanine	64	282	18048
9U ROD Crates	4	11000	44000
6U VME ROD Controller SBC	4	5000	20000
VME Trigger&Busy module	4	2000	8000
P3 Backplane	4	1000	4000
6U TTC Crate+module partitions	2	10000	20000
		TOTAL	**418048**

Table 1 ROD budget using the new integrated LArg board.

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[1] The prices shown in this table are for common orders of high quantities. E.g. S-LINK HOLA price is 282CHF for a common ATLAS order of 3000 units. But for low quantities produced and tested at CERN, 500CHF is as more realistic price. For low quantity order we could think, in general, in an increment around 25%

4 APPENDIX A: Specific Modifications for the TiCal in the LArg Motherboard Version 2.0

These are the specific hardware changes related to clock oscillators and zero ohm resistors to adapt the LArg motherboard. The rest of modifications are related with firmware which should also be developed.

- **Generate a 40 MHz clock on the G-links**
  - Remove QZ1 and QZ2 80 MHz crystal oscillator. "Or" the two resistors ROSCLLJMP1 and ROSCLLJMP2 depending of what was mounted.
  - Put on QZ1 and QZ2 a specific 40 MHz crystal oscillator.
  - It is also better to remove the R991 and ROSCLL1 resistors near the ICPLL1 device.
  - It is also better to remove the R992 and ROSCLL2 resistors near the ICPLL3 device.
- **Provide the 40 MHz clock to the PU mezzanine.**
  - Near the ICPLL1 device, on the solder side, remove the R798 and the R812 resistors.
  - Put the R814 and R815 resistors, instead.
  - Near the ICPLL2 device, on the solder side, remove the R794 and the R795 resistors.
  - Put the R799 and R800 resistors, instead.
  - Near the ICPLL3 device, on the solder side, remove the R68 and the R69 resistors.
  - Put the R71 and R72 resistors, instead.
  - Near the ICPLL4 device, on the solder side, remove the R427 and the R737 resistors.
  - Put the R743 and R746 resistors, instead.

5 APPENDIX B: A Prototype Board for Testing the Input Stage of the LArg Design

This is the design of a prototype board to check the compatibility between the FEB Interfaces Links of the TiCal and the input links of the LArg ROD. The first draft of the schematics for this card can be found at the address http://ific.uv.es/tical/rod/doc/Test_GLINK_draft.pdf

Figure 4 shows the block diagram of this design. The schematics are very similar to the LArg input stage. We use the HDMP1024 as RX, the same optical receiver and the same ACEX1k50 FPGA. Therefore with a board like this we will be able to test the input part of the LArg new design in our Valencia lab, with the only aid of a Logic Analyser to visualize the data frames received.

6 Acknowledgements

My more sincere gratefulness to all those which have helped in the smallest but important technical details and in general to the Liquid Argon and TiCal communities.

7 Acronyms

HW : Hardware

BW : Bandwidth

CB : Central barrel

CPLD : Complex Programmable Logic Device

CRC : Cyclic redundancy checking

CTP : Central Trigger Processor

DAQ : Data Acquisition (system)

DCS : Detector Control System

DCTPI : Detector-to-CTP Interface

DIG : Detector Interface Group

DSP : Digital signal Processor

EB : Extended barrel

FEB : Front end boards

FIFO : First Input First Output (memory)

FPGA : Field programmable gate array

HOLA : High-speed Optical Link for ATLAS

L1A : Level-1 Accept (Signal)

LAN : Local Area Network

LArg : Liquid Argon (calorimeter)

LDC : Link destination card

LHC : Large Hadron Collider (accelerator)

LSC : Link source card

LTP : Local trigger processor

LVDS : Low voltage differential signal

MIP : Million Instructions per Second

MUX : Multiplexer (data)

OC : Output controller (FPGA)

ODIN : Optical Dual G-LINK

PCB : Printed circuit board

PLD : Programmable Logic Device

PU : Processing unit

ROB : Read-out Buffer

RX : Link Receiver

SBC : Single Board Computer

SDRAM : Synchronous Dynamic Random Allocation Memory

SW : Software

TBM : Trigger and Busy Module

TDR : Technical design report

TTC : Timing, Trigger and Control (System)

TTCex : TTC encoder/transmitter

TTCrx : TTC receiver (chip)

TTCvi : TTC-VMEbus INTERFACE

TX : Link Transmitter

VMEbus : Versa Modular Eurocard bus

8 References

[1] **RD12 - Timing, Trigger and Control (TTC) Systems for LHC Detectors.**

Reference: http://ttc.web.cern.ch/TTC/intro.html

[2] **The I/O Dataformat for the TileCal Readout System** (J. Castelo)

Reference: http://ific.uv.es/tical/rod/doc/rod_data_format%20proposal.pdf

[3] **TileCal ROD HW Requirements and LArg compatibility** (J. Castelo).

Reference: http://ific.uv.es/tical/rod/doc/ROD_tical_HW.pdf

[4] **ROD Processing Unit Performance** (Jose Castelo).

Reference: http://documents.cern.ch/archive/electronic/other/agenda/a02281/a02281s2t8/ROD_DSP_performance.pdf

[5] **TileCal ROD pages.** *Reference*: http://ific.uv.es/tical/rod

[6] **Interface link pages.** *Reference*: http://hep.uchicago.edu/atlas/electr/electronics.html

[7] **Digitizers system pages.** *Reference*: http://www.physto.se/~ker/designreview/dr.html

[8] **Tilecal Electronics (CERN)**

Reference: http://atlasinfo.cern.ch/Atlas/SUB_DETECTORS/TILE/elec/electronics.html

[9] **Agilent HDMP-1032/1034 Transmitter/Receiver Chip Set**

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[11] **Progress on the Motherboard (April 2002).** *Author:* Daniel Lamarra, U. Geneva

Reference: http://documents.cern.ch/AGE/current/fullAgenda.php?ida=a02524

[12] **ROD Algorithm Performances using the DSP TMS320C64x.**

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Reference: http://mclaren.home.cern.ch/mclaren/atlas/conferences/ROD/ttc.pdf

[15] **TMS320C6202, Fixed-Point Digital Signal Processor.**

Reference: http://focus.ti.com/docs/prod/productfolder.jhtml?genericPartNumber=TMS320C6202

[16] **TMS320C6414, Fixed-Point Digital Signal Processor.**

Reference: http://focus.ti.com/docs/prod/productfolder.jhtml?genericPartNumber=TMS320C6414

[17] **LArg Front-end Optical Links.**

Reference: http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/larg_links/

[18] **LAr Front-end Optical Link Selection** (from Jingbo YE www page)

Dual G-LINK. *Reference*: http://www.physics.smu.edu/~yejb/atlas/documents/link_selection_docs/dual_glink_final.doc

Single G-LINK. *Reference*: http://www.physics.smu.edu/~yejb/atlas/documents/link_selection_docs/single_glink_final.doc

[19] **TM4plus1: Active S-LINK to VME64x transition module.**

Reference: http://hsi.web.cern.ch/HSI/s-link/devices/tm4plus1/

[20] **LArg ROD Demonstrator Board (DPNC196)**

Reference:http://dpnc.unige.ch/LaMarra/DPNC196/

[21] **Use of the Central Trigger Processor (CTP) and of the Timing, Trigger& Control System (TTC) for Timing and Calibration** (R. Spiwoks)

Reference: http://press.web.cern.ch/Atlas/GROUPS/DAQTRIG/LEVEL1/ctpttc/meet_tdaq_121101.pdf

[22] **TILECAL ELECTRONICS ADDRESSING SCHEME. (**K J Anderson). University of Chicago

Reference: http://hep.uchicago.edu/atlas/electr/Writeups/TTCadr.pdf

[23] **Timing receiver ASIC (TTCrx) Reference Manual**. J. Christiansen, A. Marchioro, P. Moreira, and T. Toifl. *Reference:* http://ttc.web.cern.ch/TTC/TTCrx_manual3.5.pdf

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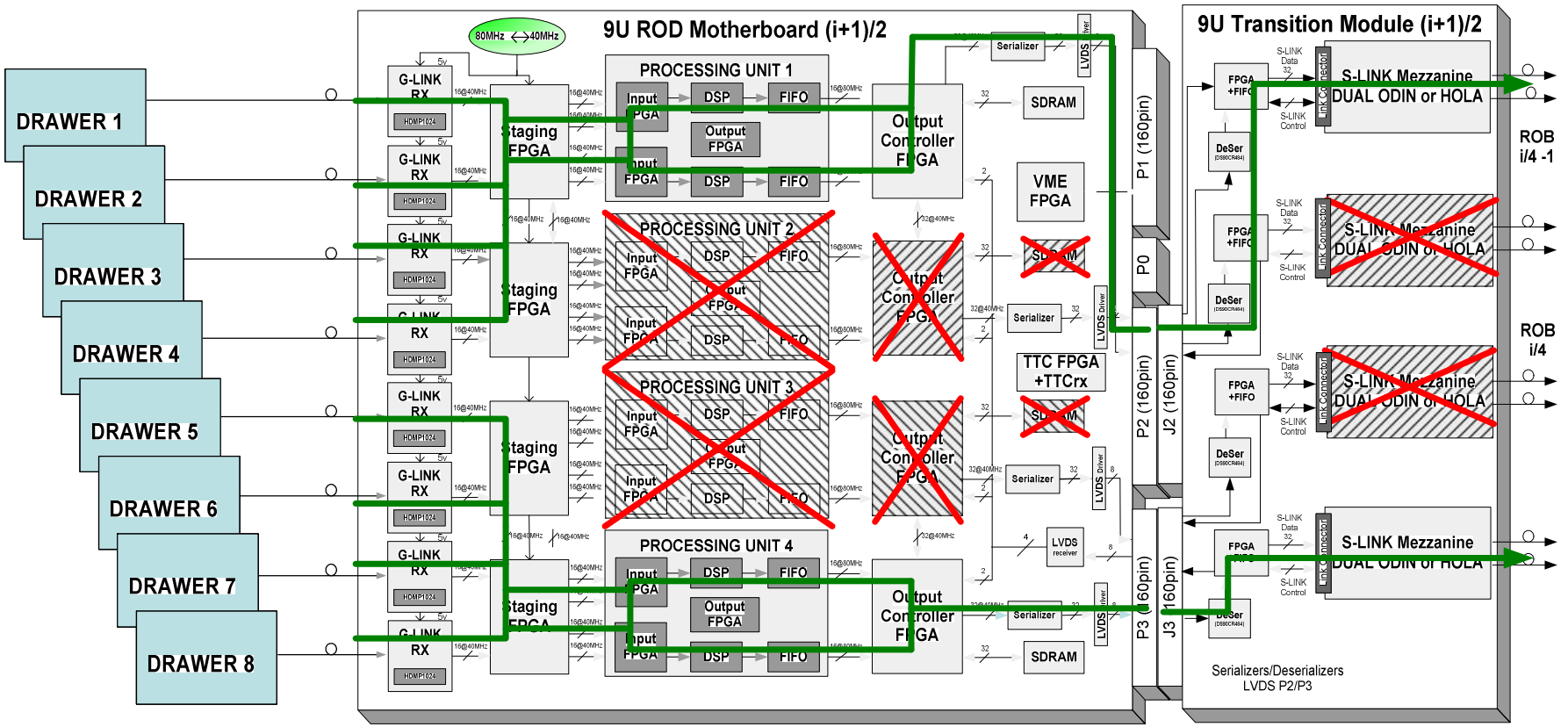

Figure 1 Dataflow of the preferred solution using new LArg motherboard

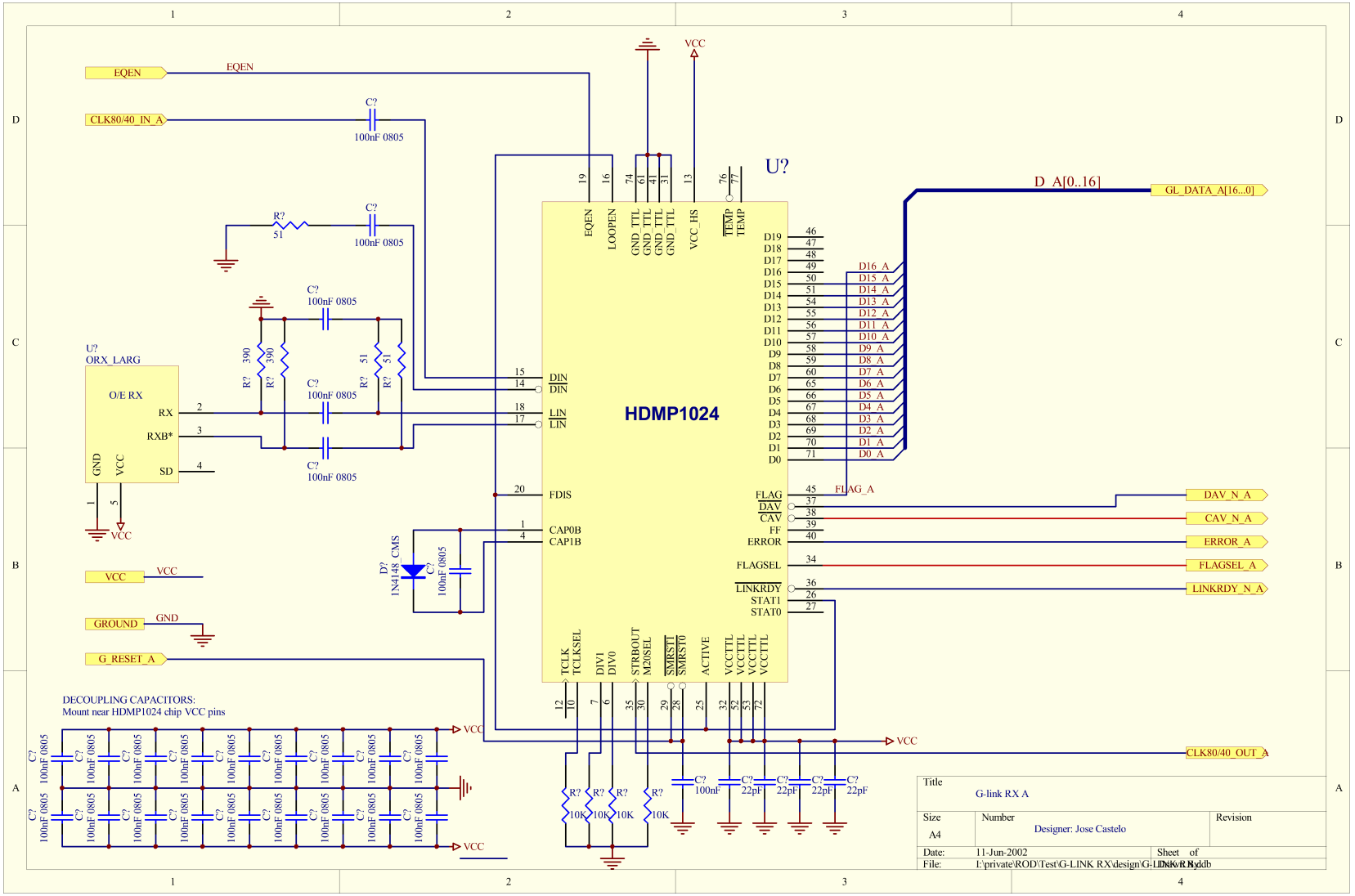

Figure 2 LArg Input GLINK. In RED is marked the CAV line

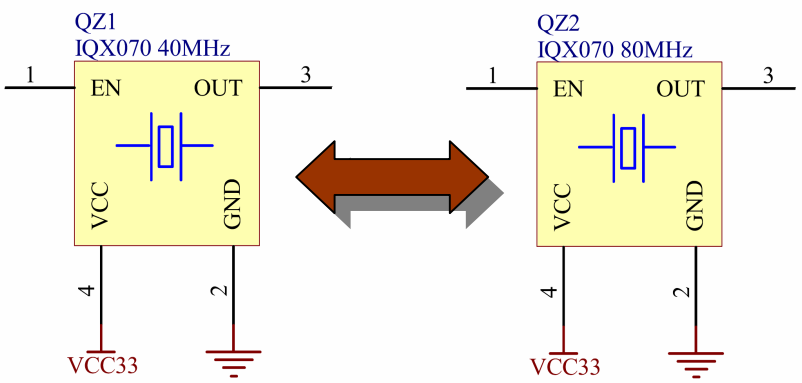

Figure 3 Interchanging the clock chips mounted in the board

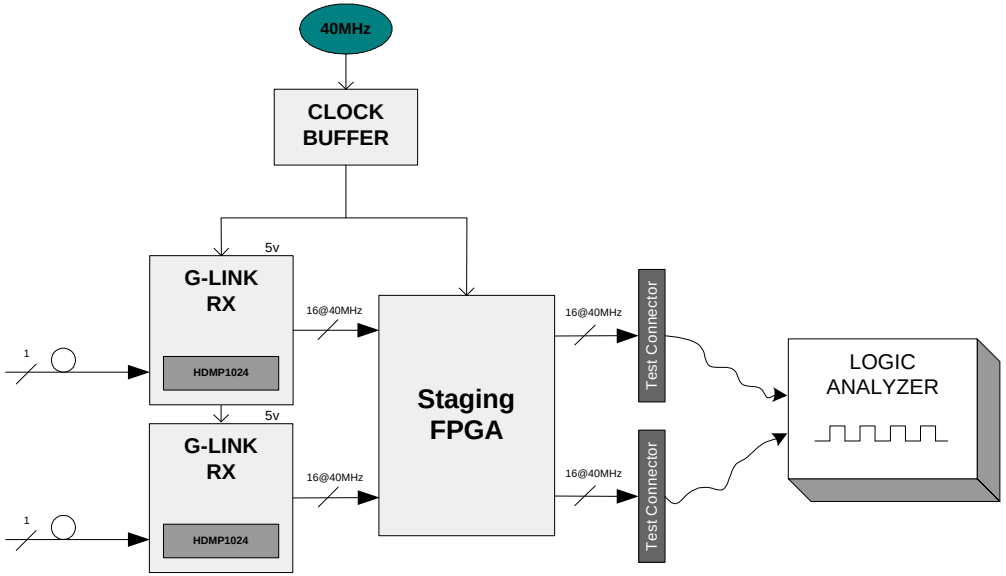

Figure 4 Test Board Block Diagram

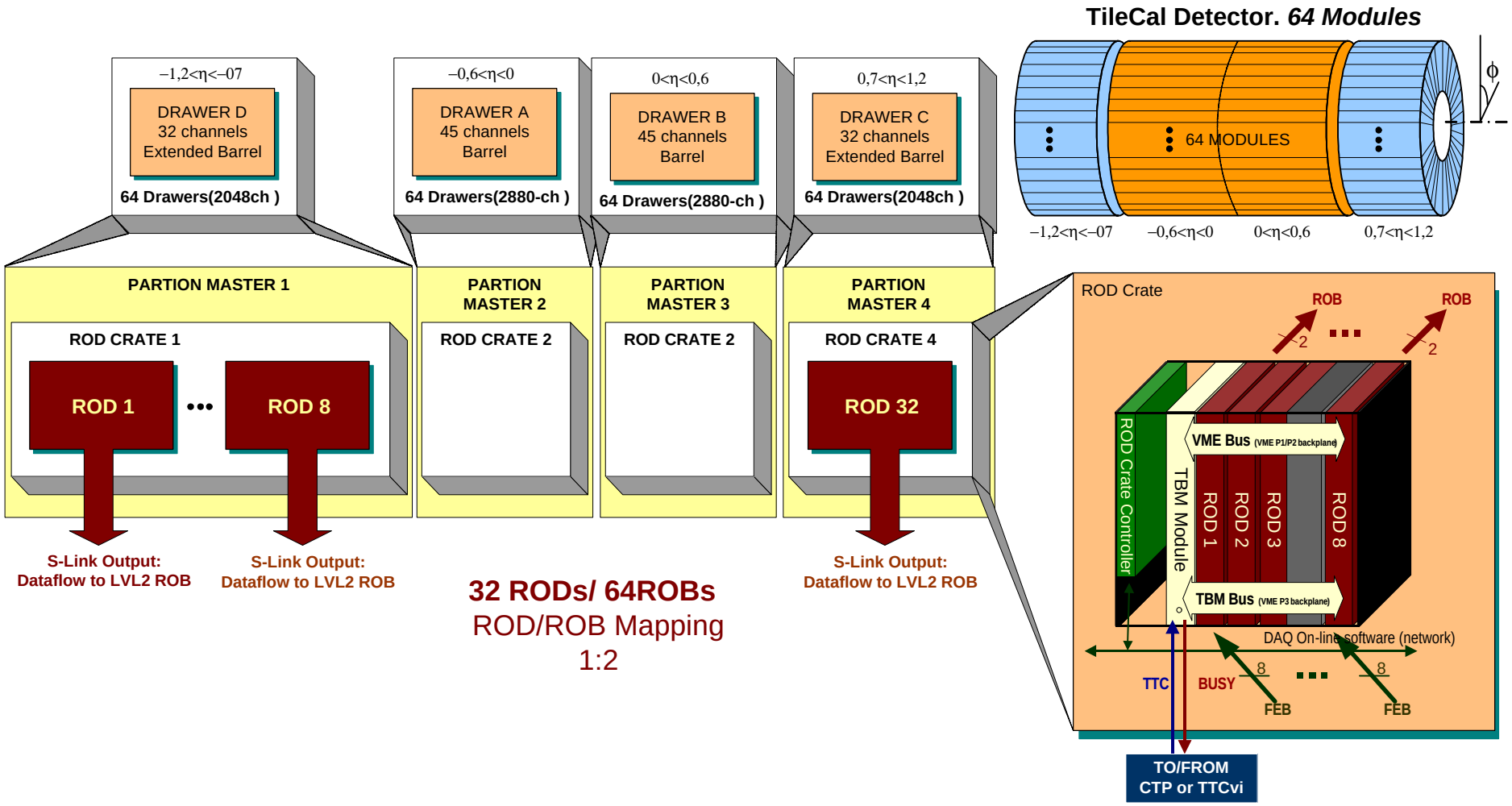

Figure 5 Preferred configuration of 4 TTC partitions in barrels