FPGA Implementation of Optimal Filtering Algorithm for TileCal ROD System

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Abstract

Traditionally, Optimal Filtering Algorithm has been implemented using general purpose programmable DSP chips. Alternatively, new FPGAs provide a highly adaptable and flexible system to develop this algorithm. TileCal ROD is a multi-channel system, where similar data arrives at very high sampling rates and is subject to simultaneous tasks. It include different FPGAs with high I/O and with parallel structures that provide a benefit at a data analysis.

The Optical Multiplexer Board is one of the elements presents in TileCal ROD System. It has FPGAs devices that present an ideal platform for implementing Optimal Filtering Algorithm. Actually this algorithm is performing in the DSPs included at ROD Motherboard. This work presents an alternative to implement Optimal Filtering Algorithm.

I. Introduction

TileCal [1] is the hadronic tile calorimeter of the ATLAS-LHC [2] experiment and consists in terms of electronic readout of roughly 10000 channels read each 25 ns. Data gathered from these channels are digitized and transmitted to the Data Acquisition System (DAQ) following a three level trigger system.

The main component of the back-end electronics of the TileCal sub-detector is the Read-Out Driver (ROD) [3], which is placed between the first and the second level trigger. The ROD has to pre-process and gather data coming from the Front End Boards (FEB) and send these data to the Read-Out Buffers (ROB) in the second level trigger.

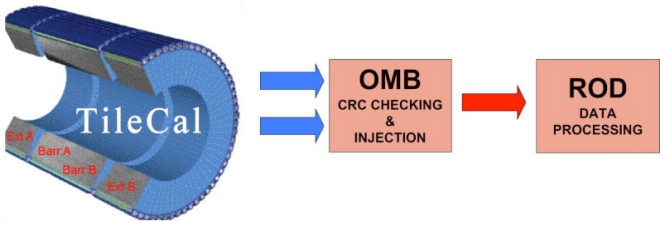

Figure 1: The OMB in the TileCal data acquisition chain.

Digital Signal Processor (DSP) is one of the main component in the TileCal Read-Out Driver (ROD) System, which receives data validated by the first level trigger. DSPs are responsible for data reconstruction in real time at the ATLAS first level trigger rate (100 KHz).

Figure 2 shows the final architecture for the acquisition chain of TileCal [4]. The Optical Multiplexer Board (OMB) will be placed in ROD crates, each OMB will receive 16 fibers from the front end of the detector and will output 8 fibers to each ROD.

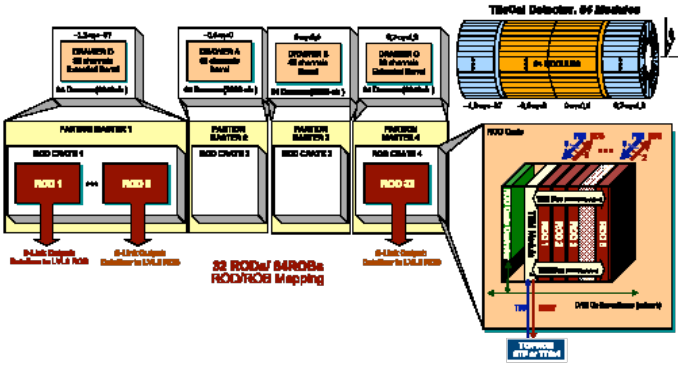

Figure 2: TileCal ROD general architecture organized around ROD crates.

The results of implementing the DSPs functionality inside the FPGAs contained in OMB 9U are described in this paper as well as the functional description and technical specifications.

II. Optimal Filtering Algorithm

The Optimal Filtering (OF) algorithm reconstructs the amplitude and phase of a digitized signal by a linear combination of its digitized samples, pedestal subtracted.

$$A = \sum_{i=1}^{n} a_i (S_i - p) \qquad (1)$$

$$\tau = \frac{1}{A} \sum_{i=1}^{n} b_i (S_i - p) \qquad (2)$$

$$\chi = \frac{1}{A} \sum_{i=1}^{n} \left| ((S_i - p) - A g_i) \right| \qquad (3)$$

where S_i represents the digital sample i and n is the total number of samples. The number of samples is 7 for physics and 9 for calibration runs [5]. We define the pedestal, p, as the baseline of the signal. The amplitude, A, is the height of the signal measured from the pedestal, τ, is the phase and it is defined as the time between the central sample and the peak of the pulse (Fig. 3).

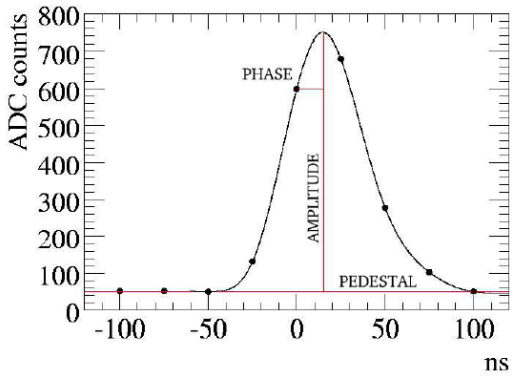

Figure 3: Definition of amplitude, phase and pedestal.

The weights, a_i and b_i, are obtained from the pulse shape of the photomultipliers and the noise autocorrelation matrix, g_i. Determine correctly weights minimize the effect of the noise in the amplitude and phase reconstruction [6].

DSP has to compute energy, phase and Quality Factor (QF) for all the channels in less than 10 us at the ATLAS maximum rate and send the reconstructed data to the second trigger level.

III. Optimal Filtering Development

Traditionally, digital signal processing (DSP) algorithms are implemented using general-purpose (programmable) DSP chips for low-rate applications, or special-purpose (fixed function) DSP chip-sets and application-specific integrated circuits (ASICs) for higher rates.

Advancements in Field Programmable Gate Arrays (FPGAs) provide new options for DSP design engineers. The FPGA maintains the advantages of custom functionality like an ASIC while avoiding the high development costs and the inability to make design modifications after production. The FPGA also adds design flexibility and adaptability with optimal device utilization while conserving both board space and system power, which is often not the case with DSP chips.

In some high-performance signal processing applications, FPGAs have several significant advantages over high-end DSP processors. FPGAs can take advantage of their highly parallel architectures and offer much higher throughput than DSPs. As a result, FPGAs overall energy consumqption may be significantly lower than that of DSP processors.

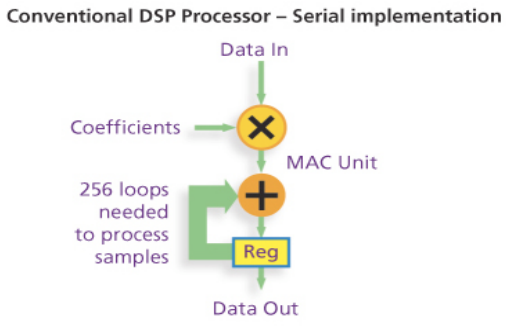

Figure 4: DSP Processor.

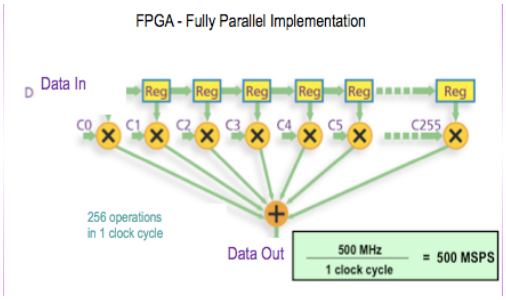

Figure 5: FPGA Implementation.

This paper presents a comparative between OF in DSP and OF in FPGAs.

A. OF in DSPs

Processing Units of the TileCal ROD have two Texas Instruments TMS320C6414 DSPs which provide an instruction cycle frequency of 720 MHz, 1024KB of user memory and an interrupt latency of 900ns. Each ROD DSP has to compute the data coming from two TileCal modules, i.e. two times 48 channels.

The Energy, Phase and Quality Factor is computed sequentially and the ROD DSP takes 8us to compute these three magnitudes for 96 channels. In addition, the DSP has to sycnhronize and to format the data.

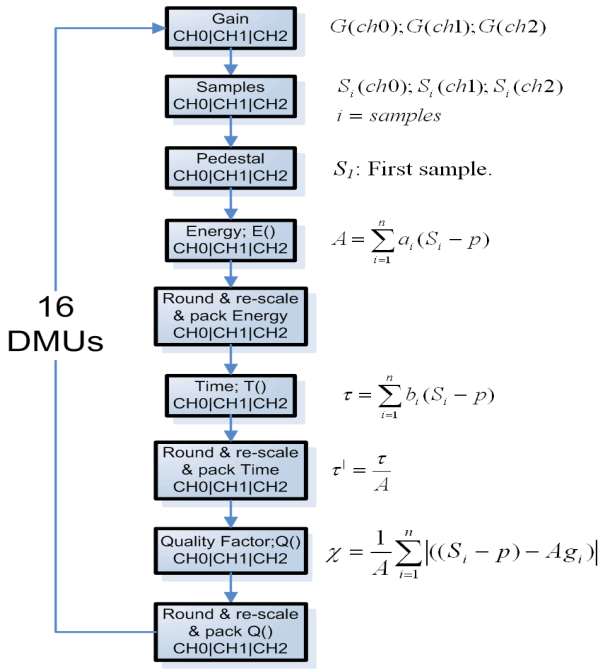

Figure 6: Optimal Filtering DSP algorithm.

The DSP performance was also tested at high event rate during the production tests [7]. The maximum Level 1 event rate can not be achieved in copy mode due to the ROD output data bandwidth limitations and in OF mode due to the OF algorithm processing time, which is 23 µs is the current DSP version. It is expect to reduce the processing time to under 10 µs by using OF without iterations and an optimized programming of the reconstruction algorithms in assembler.

B. OF in FPGAs

Another performance improvement is the ability to separate the data stream into multiple parallel blocks of data which have limited interdependence. Each data block can then be operated on independently, and the results combined, resulting in higher relative performance. Taking advantage of any architectural opportunity for maximizing the number or speed of operations is essential to maximizing the performance achievable within an FPGA [8].

In FPGAs we can generate OF Algorithm by using two methods, VHDL Blocks and Embedded DSPs. VHDL method uses separate multiplier and accumulator.

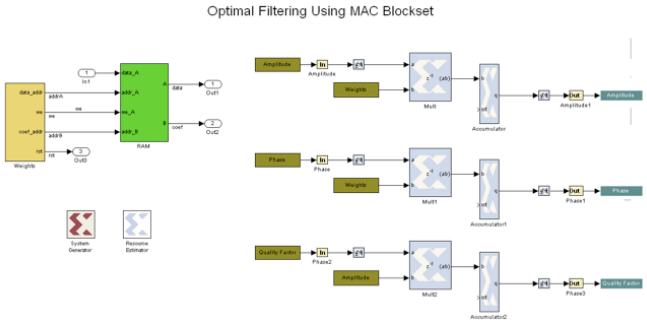

Figure 7: OF in FPGAs with VHDL Blocks.

Embedded DSP method uses hardware blocks incluyes in FPGA.

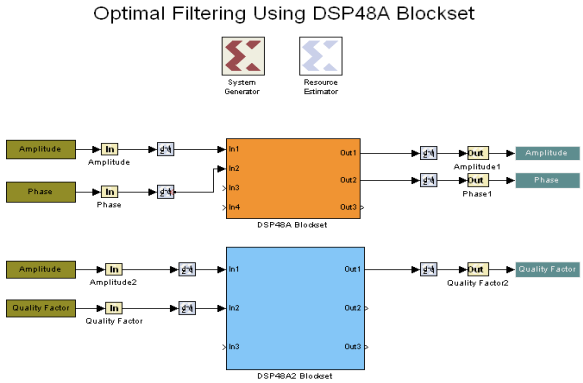

Figure 8: OF in FPGAs with Embedded DSP Blocks.

With VHDL Method we need 81 Slices and a maximum frequency of 116 MHz. With Embedded DSPs we need 25 Slices and 168 MHz. Optimal Filtering in FPGA is faster than DSPs.

IV. Conclusion

The work presented has been developed as a technology comparison between Digital Signal Processor used in TileCal RODs and new low cost FPGAs for signal processing application. The results show FPGA signal processing 100 times faster than DSPs. These results might be used in the TileCal Optical Multiplexer Boards mezzanine Processing Units if a more precise or complex reconstruction algorithm is required during the TileCal life.

V. References

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