

RoD set-up for the TileCal testbeam, 2003 period. Results and future plans.

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Abstract

During summer 2003, the Read out Driver (RoD) Demonstrator motherboard was used in a parallel data acquisition system for the ATLAS Tile Hadronic Calorimeter (TileCal) test beam.

The data chain from the front end electronics to a Read out Buffer (RoB) emulator was closed, through the RoD, with optical links. Some on-line data processing was done in the Digital Signal Processors (DSP) where different data filtering algorithms were implemented. Preliminary offline analyses show promising results.

The early future brings several exciting challenges. A small batch of the final version of RoD motherboards will be available in few months. Several tests will have to be carried out. Moreover, those boards will play a crucial role on the TileCal commissioning which is now being planned out.

I. TEST BEAM SET-UP: HARDWARE

The ATLAS Tile Hadronic Calorimeter consists of three aligned barrels. The region $-1.0 < \eta < 1.0$ is covered by the central barrel and the region of $0.8 < \eta < 1.7$ is covered by the extended barrels. All three of them are divided into 64 wedges, called modules. Each of these modules spans 0.1 rad in the polar angle [1].

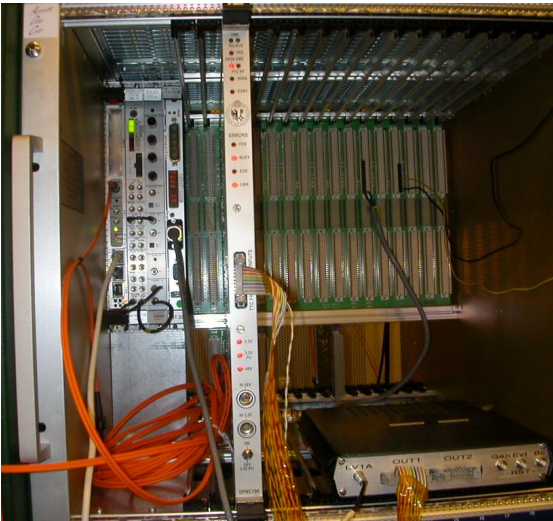


Figure 1: Front view of RoD crate. From left to right: SBC with TTCpr, TTCvi, TTCvx, VME bus tracer and the RoD Demo.

The TileCal front end electronics is divided in 256 units, called super-drawers, one per extended barrel module and two per central barrel module. These super-drawers house the photomultipliers, power distribution, signal conditioning and digitizing system and trigger related electronics.

Following the data flow, the interface card is the last piece of equipment of every super-drawer. When a “level 1 accept” is asserted, this card sends the data collected from all the photomultipliers of a given super-drawer to the RoDs, through two optical fibers.

Six super-drawers are read out in the TileCal testbeam. As no final RoD was available, a RoD Emulator system, based on two Single Board Computers (SBC) with eight ODIN cards, was introduced [2]. Six of these ODIN cards are Link Destination Cards (LDC) to read out the super-drawers. The other two, Link Source Cards (LSC), send the data to the RoB. This system does not have any processing power and only reads out one of the two fibers from the super-drawer.

However, a RoD Demonstrator motherboard (RoD Demo) [3], prototype of the final RoD motherboard, was installed in a parallel acquisition system in the 2003 testbeam period. This parallel system consisted of a 9U VME crate and a RoB emulator, see Figure 1. The crate housed the RoD Demonstrator motherboard, a transition module (TM) and a SBC with a mezzanine TTC PCI receiver (TTCpr).

One of the fibers from the interface card of a super-drawer was plugged to this RoD Demo while the other redundant fiber was connected to the RoD Emulator. This configuration did not interfere with the standard data acquisition system while the RoD Demo was debugged and set up.

The RoD Demo data flow starts in a 9U VME TM, the TM4plus1. This TM has four slots for S-Link ODIN LDC and an integrated LSC, see Figure 2. Through the J2 connector, data proceeds to the RoD Demo and, then, to a mezzanine Processing Unit (PU). In the PU, data is processed together with the trigger information.

The coincidence of three scintillators triggers the acquisition of physic events. Other trigger modes are allowed for calibration purposes, i.e., charge injection, laser or pedestal triggers. These different kinds of trigger signals are sent to the TTCvi [4], a VME module which incorporates the bunch crossing identification (BCID), level 1 accept identification (LVL1ID), trigger type (TType) and eventual commands. The TTCvi sends this trigger information to a TTCex. This module sends all the trigger information to the

super-drawers, the RoD Emulator and the RoD crate, through optical link.

The TTCpr, in the RoD crate, receives and decodifies the trigger information from the TTCex. The SBC, on which the TTCpr is mounted, sends this trigger information to the RoD Demo through the VME bus. The VME FPGA, interface of the VME bus and the RoD Demo, routes trigger information to the TTC FPGA, which sends it to the Output controller FPGA and to the Input FPGA on the PU.

Processed data is sent back to the TM from the PU. The integrated LSC links to the RoB emulator which consists in a PC with an ODIN LDC mounted on a S-Link to PCI interface, the S32PCI64. The main features of this PC are fast Ethernet connections and 64bit PCI buses. All the data is transferred to the 64 bit PCI bus. This computer acts, as well, as gateway to the SBC and to the VME bus. Data is collected and stored in the hard drive of the RoB Emulator.

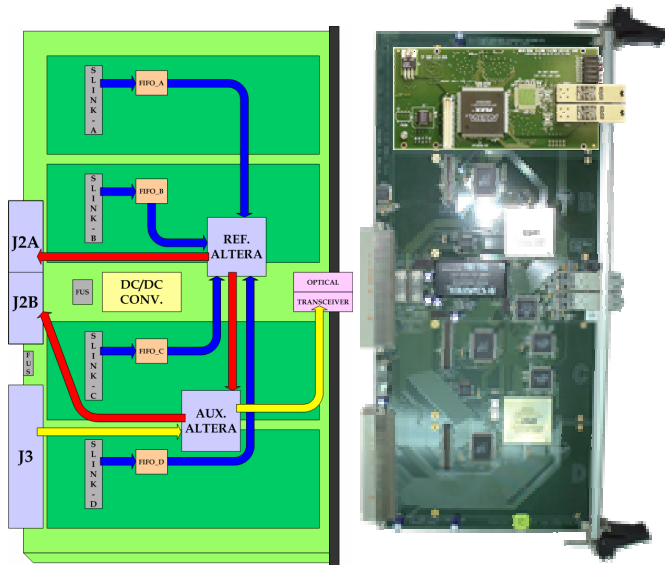


Figure 2: Left: TM4plus1 data flow. Right: Picture of the TM4plus1 with a LDC.

II. TEST BEAM SET-UP: SOFTWARE AND FIRMWARE

Several devices required programming for this set-up: two FPGAs on the TM (reference and auxiliary), Input FPGA and DSP in the PU and the FPGA in the motherboard. Software development was needed, also, for the SBC and RoB Emulator.

A. Transition Module

Two FPGAs control the data flow in the TM4plus1. The auxiliary FPGA, as a part of the integrated LSC, gets the output data from the RoD Demo and implements the S-Link protocol. The reference FPGA reads the FIFOs, on which the LDCs write input data, and sends that data to the RoD Demo.

B. RoD Demonstrator motherboard

The firmware for the the FPGAs on the RoD Demo was developed by the Liquid Argon system RoD team. The codes developed allowed a wide range of different data flow configurations, so no changes had to be done on any of these FPGAs.

C. Processing Unit

Two devices in the mezzanine PU card required programming:

1) Input FPGA:

This device, mounted on the PU, receives front end data from the TM and trigger data from the TTC FPGA. The code, synthesized for this Altera FLEX10 FPGA, collects and buffers front end and trigger data and formats it on event blocks. Then, it writes these blocks on a dual port RAM, so that the DSP can access and process data.

2) DSP

A variety of codes have been tested on the DSP, both on C++ and Assembler and with different functionalities. First versions just passed data by. Later, on-line processing functions for flat filtering (FF) and optimal filtering (OF) were included [5]. The accuracy of the calculations was the main goal during this set-up, as the time constraints were relaxed by the low event rate.

D. Single Board Computer

A modified application from the Trigger and Data Acquisition, TDAQ, software release sends the trigger information extracted by the TTCpr to the RoD Demo, using the VME libraries in the same release. This application runs on the SBC, which remote boots from the RoB emulator workstation.

E. RoB Emulator

An industrial PC on a 4U box was used as RoB Emulator and control computer. It ran under Linux and provided the operating system to the SBC. A modified application from TDAQ release used FILAR drivers for the S32PCI64 card to read and store all the data from the RoD Demo [6]. This program dumps all the data to binary files for later analysis.

III. DATA ANALYSIS

A final check of the RoD motherboard functionality consists in the comparison of the output from the on-line processing in the DSP and the off-line analysis of raw data. The off-line analysis was performed with C++ libraries on ROOT environment.

Data was taken in the late August 2003 run. Two algorithms were applied: FF and OF. Only preliminary results were available at the time of writing this paper. Histograms of the difference of the results of the on-line and off-line calculations for photomultiplier number 16 of the positive side of the central barrel are shown in Figure 3.

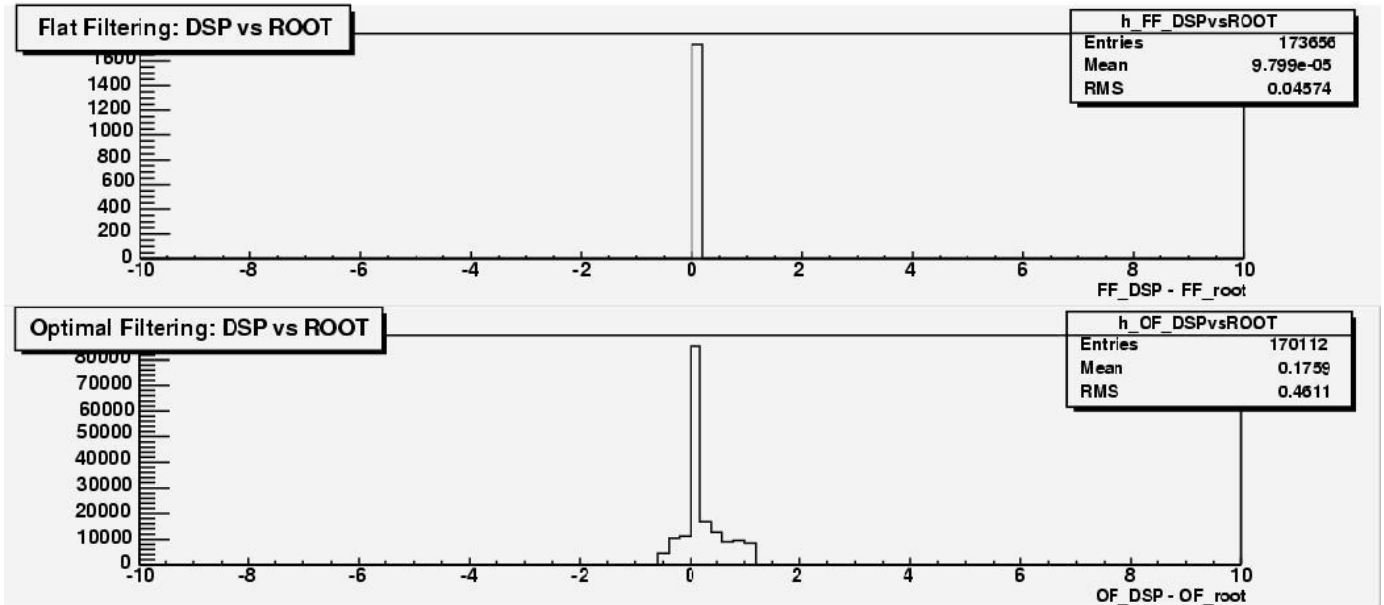


Figure 3: Histograms of the difference of on-line and off-line calculation for FF and OF.

A. Flat Filtering

This algorithm sums all nine raw data samples of one event. It is a simple algorithm to implement in the DSP and very quick to compute. The top histogram in Figure 3 shows that there are no differences in the on-line and off-line energy reconstruction.

B. Optimal Filtering

Optimal Filtering is a more sophisticated data filtering method. It requires a careful implementation in the DSP because it uses coefficients for scaling the different samples. The implementation of this algorithm involves sensitive operations like truncation and rounding up. As it is seen in Figure 3, differences appear between the on-line and the off-line calculations, mainly due to the usage of different kinds of variables and operators. Even so, those differences are below 2 ADC counts.

IV. TILECAL COMMISSIONING AND THE RODS

As the pre-assembly of the central barrel approaches completion, the TileCal collaboration gets ready to test the system with cosmic muons. A set of scintillators will trigger data acquisition. It will consist of two scintillators placed by the geometrical centre of the barrel, which, operated in coincidence, will cover an area of four modules (4×0.1 rad) and ten towers ($2 \times 5 \times 0.1$ in pseudo rapidity). First calculations result in an expected event rate from 1 to 100 Hz.

The commissioning set-up is an intermediate step between the testbeam set-up and the final ATLAS integrations. It will be a challenging experience as final RoD motherboards will

be used for the first time to read real data from twelve super-drivers.

Notwithstanding the lack of hardware, the RoD system for cosmic muons commissioning will not use PUs or TMs at the beginning. A special configuration has been designed for this period. The staging FPGA will divert data to the VME FPGA, instead of trying to inject it to the PU. Then, data will be read through VME bus.

The optical output will be tested when Transition Modules become available. The PUs, as well, will be added later on. Once PUs are on place, the RoD will have some processing power, which will be used to test several data filtering algorithms. Finally, commissioning will be a full scale test of all the TileCal system, including the Read out Driver in its final configuration.

V. REFERENCES

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- 2- <http://hsi.web.cern.ch/HSI/s-link/>
- 3- Sanchis E, Castelo J, González V, Torres J, Torralba G, Martos J, On the developments of the Read Out Driver for the ATLAS Tile Calorimeter; 7th Workshop on Electronics for LHC Experiments LEB 2001
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