Real Time Data Acquisition with Read Out Driver System

J. Torres, V. González, J. Soret, E. Sanchis, J. Martos, J. A. Gómez
Dept. Ingeniería Electrónica, Universidad de Valencia – ETSE

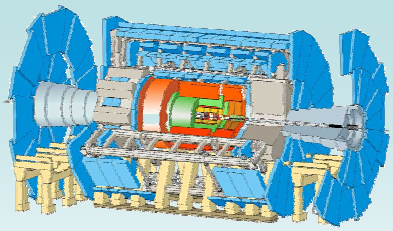
C. Cuenca, A. Ferrer, E. Fullana, E. Higón, J. Poveda, A. Ruiz, B. Salvachúa, C. Solans, J. A. Valls, J. Castelo
I.F.I.C. – Centro Mixto Universidad de Valencia – C.S.I.C.

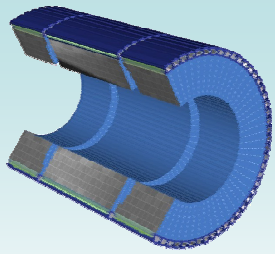
This work describes the present status and future evolution of the Real Time Data Acquisition with Read Out Driver System for the ATLAS Tile Calorimeter.

The CERN (European Laboratory for Particle Physics) in Geneva is working in new particle physics research. To develop this research, a new accelerator, the *Large Hadron Collider (LHC)* is presently being constructed. In the year 2007 beams of protons are expected to collide at a centre of mass energy of 14 TeV. In parallel to the accelerator, two general purpose detectors, *ATLAS (A Toroidal LHC Apparatus)* and *CMS (Compact Muon Solenoid)*, are being developed to investigate proton-proton collisions at this new energy domain and to study fundamental questions of particle physics.

Each detector is composed of several subdetectors, TileCal is one of these. They are prepared to read, in each collision and through thousands of electronic channels, a high data volume. Therefore, to make the integrated analysis of all their information it is necessary new real time systems. The work we present here is included in the studies and development currently carried out at the University of Valencia-IFIC for the Read Out Module (ROD) of the hadronic calorimeter TileCal of ATLAS.

ATLAS and TileCal Description





TileCal is the hadronic calorimeter of the ATLAS experiments. It consists, electronically speaking, of ~10000 channels to be read each 25 ns. Data gathered from these channels are digitized and transmitted to the data acquisition system (DAQ) following the assertions of a three level trigger system. In the acquisition chain, place is left for a module which has to perform preprocessing and gathering on data coming out after a good first level trigger before sending them to the second level.

This module is called the Read Out Driver (ROD) and is built around custom VME boards. The ROD has thus to cope with a maximum input data bandwidth of 14 Gbytes/sec and an output bandwidth of 6.7 Gbytes/sec at the expected 100 kHz ATLAS level 1 trigger rate.

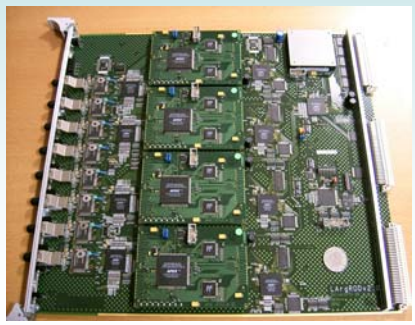
ROD

There will be a total of 32 ROD VME64x boards to read the whole TileCal detector, with up to four PUs (Processing Units) each.

A basic list of the ROD functionalities include:

- To receive, process and check data consistency from the FEBs (Front-End Buffers) through eight optical fibers.
- To calculate energy and time through an optimal filtering method at the PU DSP (Data Signal Processor) level. The result is sent to the ROB (Read-Out Buffer) modules where this information is made available for subsequent trigger decisions.
- To monitor the data to ensure a good quality data logging.
- To generate BUSY signals to the CTP (Central Trigger Processor) in case of problems in the data treatment by the DSPs.

The RODs operate an optical-to-electrical conversion through optical receivers and ensure full compatibility with the FEB output data format.



Due to the reduced channel density of the TileCal with respect to the LiAr calorimeters, the TileCal RODs can operate with 50% of the PUs and S-Link outputs (the RODs support up to four S-Link output mezzanine cards called Link Source Cards).

The core of the ROD motherboard are the four PUs mounted as mezzanine boards (120×85 mm) on them. These mezzanine are composed of two DSP blocks each, able to treat up to 128 channels (LiAr RODs) or up to 45 channels (TileCal RODs) operating in normal mode. Each DSP block is composed of an input FPGA, a TMS320C6414@600 MHz DSP from Texas Instruments and an output FIFO. The mezzanine also contains an output FPGA used for the VME and TTC interface of the ROD. The input bandwidth of the PU is 2.5 Gbits/sec (64 bits@40 MHz) which is enough to cope with the expected input stage bandwidth on the ROD. The current choice of DSP provides sufficient flexibility to choose between different schemes in data processing.

The main functionalities of the PUs can be summarized as:

- Dataflow management, data formatting, TTC (trigger) reception, buffering and synchronization.
- Data processing with reconstruction algorithms.
- Error detection.

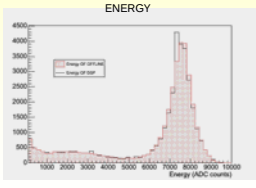
DSP Simulation Test Results

Recent studies have proved the implementation and performance of Optimal Filter (OF) energy and time reconstruction algorithms simulating the operation of the DSPs. The TMS320C64x DSP family has an architecture specifically designed for real time processing with up to eight 32-bit instructions per cycle (6000 MIPS). The device is only able to operate with MAC instructions as its CPU contains multiplier and ALU units. Divisions are not allow and only SSH instructions can be implemented.

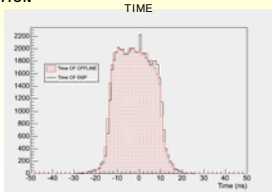
The precision achieved with these implementations at the DSP level are similar to those obtained with an offline implementation, in all cases with TestBeam data. The plots below show a comparison of the offline and online DSP implementation of the reconstructed energy and time using OF algorithms from 2003 TestBeam data.

OPTIMAL FILTER
1 ITERATION

ENERGY



TIME



Optical Multiplexer Board

TileCal is a redundant data acquisition system. Two optical fibers carry the same data from the front-end electronics to the ROD. This is necessary because of radiation phenomena which could cause malfunctions inside the front-end electronics, and bit and burst errors over data ready to be transmitted to the ROD card.

Our primary target is to improve error tolerance, designing a pre-ROD card, called Optical Multiplexed Board (OMB), able to analyze two fibers, both of them carrying the same data, to provide the correct one to the ROD input.

The construction of a OMB first prototype is finished. The verification has been realized at CERN this summer. The next step is the development of a new 9U prototype. A new functionality for OMB was proposed, which consists in the implementation of a new operation mode called “Data Injector Mode”, to use the OMB like data pattern injector towards ROD for test and verification uses.

The present ATLAS combined TestBeam at CERN is operating with different subdetectors associated to a complete wedge of ATLAS. Data is being acquired for most of them with next-to-final production RODs. In particular, the TileCal modules are being readout satisfactory with a production ROD instrumented with 3 FPGA PUs with two FEB links each. Operation with final DSP PUs is expected before the end of the run, where the simulation results above will be validated with real data operation.

IEEE-NPSS ROME 2004
Nuclear Science Symposium