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TileCal beam test read-out with RoD Demo

Castelo,Jose; Cuenca,Cristobal; Fullana,Esteban; Higon,Emilio; Salvachua,Belen; Valls,Juan
IFIC, TileCal group, Valencia Spain

Abstract

The ATLAS Tile Calorimeter (TileCal) Read-out Driver (RoD) modules are 9U VME cards which are in charge of reading and computing data from the TileCal front end electronics boards (FEB). The RoD motherboard has four mezzanine Processing Units (PU) cards, with a digital signal processor (DSP) implemented with energy and time reconstruction algorithms. The board also contains several FPGA ASICs for input/output data management and VME protocol controlling. The cards are inserted in standard 9U VME crates. They receive data through optical fibres from the FEB and send them to a Transition Module (TM) installed at the back of the VME crate.

During the summer 2003, a prototype design of the RoD for the Tile Hadronic Calorimeter of ATLAS, the RoD Demonstrator board, was integrated in a parallel data acquisition system for the TileCal beam test. The standard data acquisition system was used for the official data taking using RoD Emulators, while the RoD Demo was debugged and tested in parallel to data taking.

The beam test was performed in the north area, Prévessin, at CERN. Two central barrel modules and two extended barrel modules were targeted by the beam line from the SPS. Each half-barrel module and each extended barrel module has a super-drawer which contains all the front end and digitizing electronics. Our aim was to read one super-drawer (FEB) with one RoD Demo and one Processing Unit and study its performance. An industrial rack PC with an S-link to PCI card was used to store the data and used as a RoB (Read-out Buffer) Emulator.

Two optical fibres came out with redundant information from the FEB, and only one was used for the RoD Emulator, so, the new set-up took the second fibre without disturbing the standard beam test acquisition. Data from the FEB were received with an S-link ODIN link destination card (LDC) whose firmware was modified in order to work with the TileCal FEB interface link custom protocol based on the G-link chip HDMP1032. This ODIN LDC was mounted in the Transition Module in the rear part of the VME crate. It sent the data to the RoD Demo motherboard through the P2 backplane. Data were processed in the DSP of the PU and sent again to the transition module through a custom P3 backplane. The Transition Module had an integrated ODIN link source card (LSC) which sent the data to the RoB Emulator and dumped to a binary file for later storage and analysis. The RoB Emulator is a system made up of a workstation (the industrial rack PC) with an S-link to PCI interface card (S32PCI64 + ODIN LDC).

All VME modules were controlled with a single board computer (SBC) from Concurrent Technologies. It ran a standalone application which configured the RoD Demo motherboard and booted the PU through VME. The SBC also received TTC (trigger and control) information and sent it through VME to the RoD Demo motherboard.

Optimal Filtering and Flat Filtering algorithms were implemented in the PU for the online reconstruction of the energy and arrival time of the calorimeter signals. Online processing was unthinkable with the old set-up (RoD Emulator) based on commercial CPUs due to the lack of enough processing power.

The Flat Filtering algorithm is a very fast and simple method to estimate the energy and consists in adding the energy of all signal samples. The Optimal Filtering method allows a better reconstruction of timing and amplitude by optimizing the energy reconstruction minimizing the noise.

Offline data have been analysed in order to check the implementation of the algorithms in the DSP with satisfactory results.