TileCal beam test Read-out with RoD Demo

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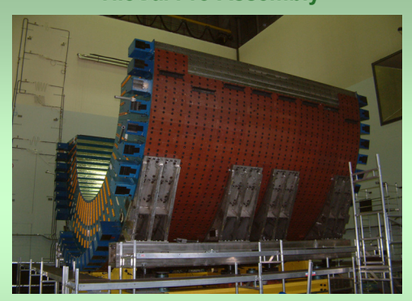
The ATLAS Hadron Tile Calorimeter (TileCal) Read-out Driver (RoD) modules are 9U VME cards which are in charge of reading and computing data from the TileCal front end electronics boards (FEB). The RoD motherboard has four mezzanine Processing Units (PU) cards, with a Digital Signal Processor (DSP) implemented with signal energy and time reconstruction algorithms. The board also contains several FPGA ASICs for input/output data management and VME protocol controlling. The cards are inserted in standard 9U VME crates. They receive data through optical fibres from the FEB and send them to a Transition Module (TM) installed at the back of the VME crate.

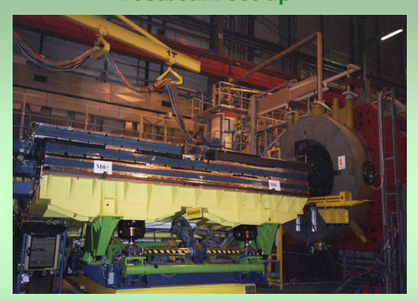
During the summer 2003, a prototype design of the RoD for the Tile Hadronic Calorimeter of ATLAS, the RoD Demonstrator board, was integrated in a parallel data acquisition system for the TileCal beam test. The standard data acquisition system was used for the official data taking using RoD Emulators, while the RoD Demo was debugged and tested in parallel to data taking.

The beam test was performed in the north area, Prévessin, at CERN. Two central barrel modules and two extended barrel modules were targeted by the beam line from the SPS. Each half-barrel module and each extended barrel module has a super-drawer which contains all the front end and digitizing electronics. Our aim was to read one super-drawer (FEB) with one RoD Demo and one Processing Unit and study its performance. An industrial rack PC with an S-link to PCI card was used to store the data and used as a RoB (Read-out Buffer) Emulator.

TileCal Pre-Assembly



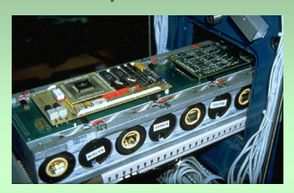
Testbeam set-up



ATLAS Tile Hadronic Calorimeter consists of three aligned barrels each one azimuthal divided into 64 modules. The hole calorimeter covers the region of $-1.7 < \eta < 1.7$.

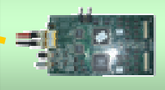
During the beam test the four modules are on a mobile table which allowed to scan them in several directions in η.

Super-drawer



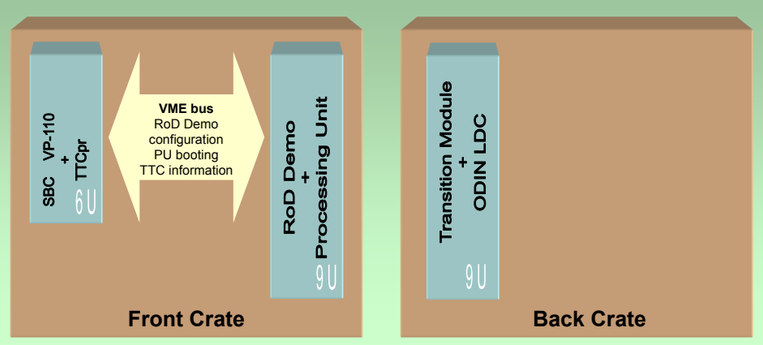
There are 256 super-drawers covering the whole Tile Calorimeter. The super-drawers are situated inside the back-beam region of the calorimeters and houses up to 24 pairs of PMT's.

Interface card



Following the data flow, the interface card is the last piece of equipment of every super-drawer. When a "level 1 accept" is asserted, this card sends the data collected from all the photomultipliers of a given super-drawer to the RoD, to optical fiber.

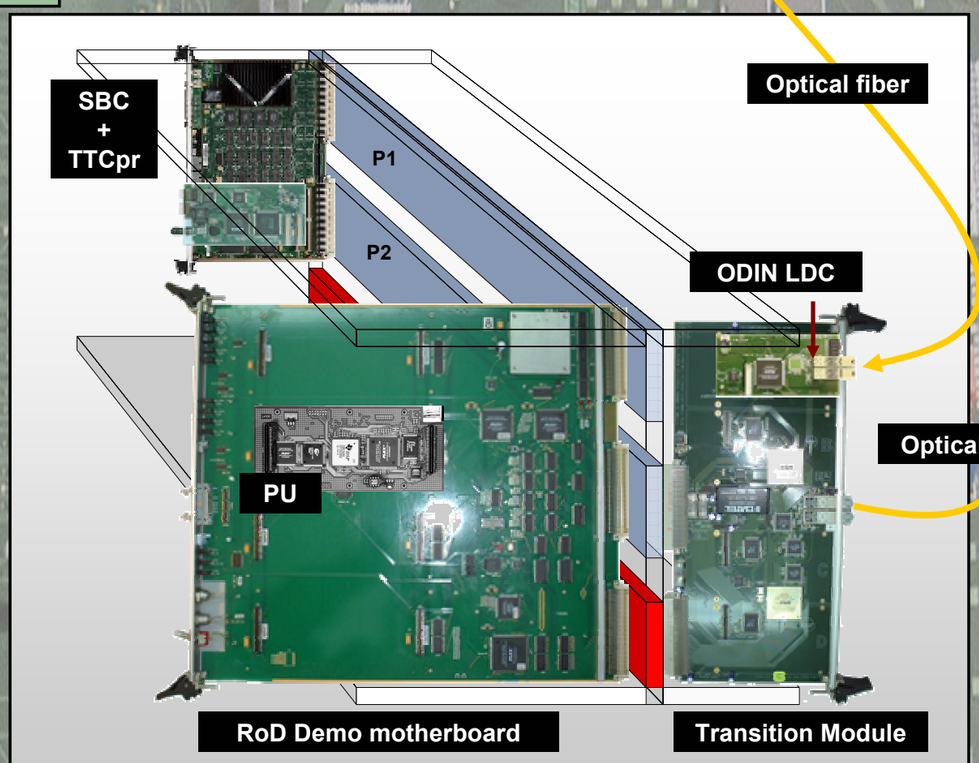
RoD Demo Crate description



An ATLAS standard VME single board computer (SBC) VP-110 from Concurrent Technologies makes the functions of a RoD controller.

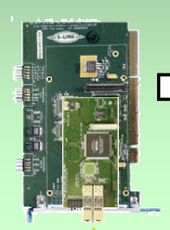
This CPU boots Linux Kernel and filesystem using DHCP and NFS protocols respectively from the ROB Emulator. The RoD controller runs a standalone application which configures the slave VME module (RoD Demo motherboards) and boots the PU through VME bus.

Concerning the Timing and Trigger Control (TTC) information, there is a PMC board called TTCpr mounted in the SBC. This card has basically an optical receiver, a TTCrx chip to decode TTC multiplexed information and a PCI bridge. The RoD controller reads continuously the TTC information when it is available and sends it through its VME bridge chip to trigger the slave RoD Demo module.

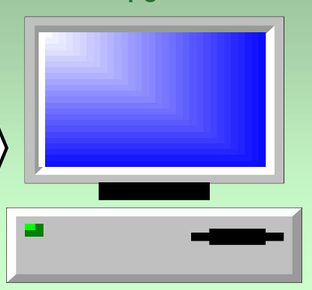


Data from the FEB are received with a S-link ODIN link destination card (LDC) whose firmware was modified to cope with the TileCal FEB interface link custom protocol based on g-link chip HDMP1032. This LDC is mounted in a transition module in the rear part of the crate. It sends data to the RoD Demo motherboard through the P2 backplane. Data are processed in the DSP (Digital Signal Processor) of the PU and sent again to the transition module through a P3 custom backplane. The transition module has an integrated ODIN link source card (LSC) which sends the data to the RoB Emulator.

S32PCI64 + ODIN LDC



PC



The RoB Emulator consists of an industrial rack PC with a S-link to PCI interface card (S32PCI64 + ODIN link destination card LDC). Data from the Transition Module are received with the ODIN LDC and sent to the PC through the S32PCI64 card to be dumped to binary files. Then these files are stored in a secure place for offline analysis.

The Tile Calorimeter read-out is based on a fast digital sampling of a shape waveform. Commercial ADCs (Analog Devices ADC9050@40MHx) are used for sampling the signal. Two shapes of the same signal are digitized, one for low gain and another one for high gain (amplified a factor of 64). The inputs of the RoD are signals with 7 or 9 samples and high or low gain, except if a calibration mode is set, in which case both gain signals are sent to the RoD.

For the present analysis a normal operation mode with 9 samples signals were chosen. A header before the data indicates if the signal from one PMT channel was sent in high or low gain.

OPTIMAL FILTERING ALGORITHM

Optimal Filtering algorithm allows a good reconstruction of timing and amplitude from calorimeters multiply-sampled shaped signals minimizing the noise.

The advantage of this method is the reduced sensitivity to channel-to-channel variations.

Linear combinations of the samples are used in order to recover the signal parameters, *Start time* (τ) and *Amplitude* (A).

DSP IMPLEMENTATION

The Processing Units are provided with a fixed point DSP of Texas Instruments where the algorithms run. There are not MAC instructions available in such DSPs so only sums (ADD) and multiplications (MPY) have to be implemented. For this first version of the firmware some divisions are implemented as shift instructions (SSH) or using look-up tables in order to reduce processing time.

The Implementation of Flat Filtering on the DSP is equal to the implementation on a floating point processor but the algorithm of Optimal Filtering is quite different as described below.

Samples coming from the front end electronics:

$S_1\ S_2\ S_3 \ldots S_n$

First Set of weights, for amplitude calculation:

$a_1\ a_2\ a_3 \ldots a_n$

Second Set of weights, for start time calculation:

$b_1\ b_2\ b_3 \ldots b_n$

What does *Amplitude* mean?

The ***Amplitude*** of the signal is proportional to the Energy deposited on the detector.

$$A = \sum_{i=1}^{n} S_i \cdot a_i$$

$$A \cdot \tau = \sum_{i=1}^{n} S_i \cdot b_i \quad \Rightarrow \quad \tau = \frac{1}{A} \sum_{i=1}^{n} S_i \cdot b_i$$

What does *Start time* mean?

Start time or ***Phase*** is the distance in time between the maximum sample and the maximum of the shape form.

$$A_i = a_i \cdot 2^{15}$$

$$B_i = b_i \cdot 2^{10}$$

$$A = \left(\sum_{i=1}^{N^\circ samples} A_i \cdot S_i - p \sum_{i=1}^{N^\circ samples} A_i \right) \cdot 2^{-15}$$

$$\tau = \frac{1}{A} \left(\sum_{i=1}^{N^\circ samples} B_i \cdot S_i - p \sum_{i=1}^{N^\circ samples} B_i \right) \cdot 2^{-10}$$

Originally the weights a_i and b_i are 32 bits words treated by a floating point processor. This processor scales the coefficients to the maximum allow in order to work with integers of 16 bits. The new weights are passed to the DSP at boot time.

Pedestal (*p*) is calculated as the sum of the first sample and the last sample divided by two. This division is made as a right shift of one bit.

Amplitude **and** ***Start time*** **are calculated with the new coefficients and then normalized again by shifting right the result in 15 and 10 positions respectively.**

FLAT FILTERING ALGORITHM

The Flat Filtering algorithm is a very fast and simple method to estimate the energy adding all signal samples.

Samples coming from the front end electronics:

$S_1\ S_2\ S_3 \ldots S_n$

$$E \propto \sum S'_i$$

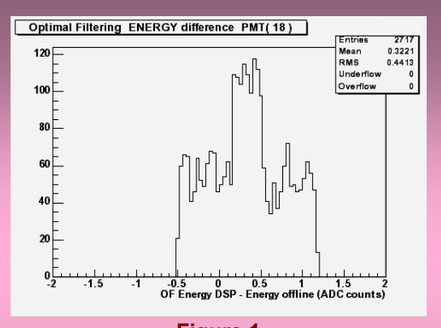


Figure 1

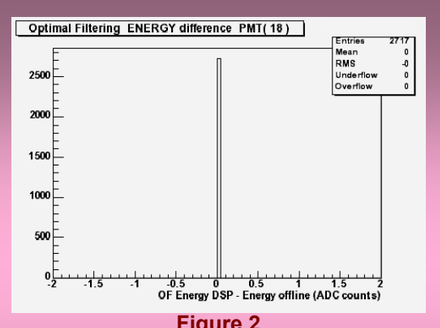


Figure 2

Figure 1 shows the difference between the Amplitude calculated online in the DSP and the Amplitude calculated offline, working in floating point and with 32 bits words.

Figure 2 shows the difference between the Amplitude calculated online in the DSP and the Amplitude calculated offline, using the same approximations made in the DSP such as working with integers of 16 bits, scaling the weights, rescaling the Amplitude and using shift instructions instead of divisions.

References:

"Data acquisition system (RoD) for the Tile hadronic Calorimeter. Testbeam installation" *J. Castelo*, Research report.
"Optimal Filtering applied to 1998 Test Beam of Module 0" *F. Camarena, J. Castelo, E. Fullana* ***(ATL-TILECAL-2002-015).***
"RoD set-up for the TileCal testbeam, 2003 period. Results and future plans" *J. Castelo, C. Cuenca, E. Fullana, E. Higón, B. Salvachúa, J. Torres. (Contribution to* ***LEEC 2003****: 9th Workshop on Electronics for LHC Experiments).*
For more detail see: **http://ific.uv.es/tical/rod/**