The Optical Multiplexer Board for the ATLAS Hadronic Tile Calorimeter

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***Abstract*–This paper presents the architecture and the status of the Optical Multiplexer Board (OMB) for the ATLAS/LHC Tile hadronic calorimeter (TileCal). This board will analyze the front-end data CRC to prevent bit and burst errors produced by radiation. Besides, due to its position within the data acquisition chain it will be used to emulate front-end data for tests. The first two prototypes of the final OMB 9U version have been produced at CERN. Detailed design issues and manufacturing features of these prototypes are described. These prototypes are being validated while firmware developments are being implemented in the programmable devices of the board.**

I. Introduction

TILECAL [1] is the hadronic calorimeter of the ATLAS-LHC [2] experiment and consists in terms of electronic readout of roughly 10000 channels read each 25 ns. Data gathered from these channels are digitized and transmitted to the Data Acquisition System (DAQ) following a three level trigger system (Fig.1).

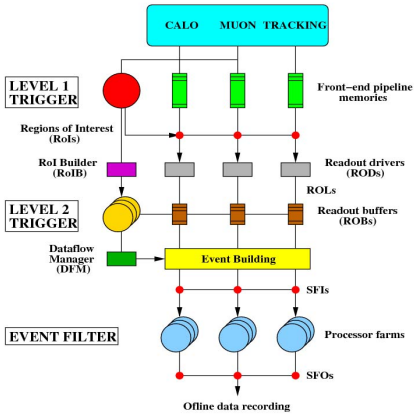

Fig. 1. The ATLAS three levels trigger system.

The main component of the back-end electronics of the TileCal sub-detector is the Read-Out Driver (ROD) [3] which is placed between the first and the second level trigger level. The ROD has to pre-process and gather data coming from the Front End Boards (FEB) and send these data to the Read-Out Buffers (ROB) in the second level trigger.

TileCal electronics will receive about 2 Gy/year (0.2 Krad/year) of radiation for a total dose of 20 Gy in the experiment lifetime [4]. To measure radiation hardness of TileCal FrontEnd electronics, tests were conducted with proton beams in different areas and with different beam sizes. Thanks to these tests, three non-destructive kinds of errors were found:

- Transient error in the data flow out to the ROD.
- Permanent errors in the data flow requiring reset.
- Latch-up error with an increment in current consumption of 60 mA.

To reduce data loss due to radiation effects, the TileCal collaboration decided to include data redundancy in the output links of the FrontEnd. This was accomplished using two optical fibres which transmit the same data. At ROD system level, data redundancy is used to discard the fibre with errors due to radiation. The checking is based on rightness of the Cyclic Redundancy Codes (CRC) of the data packets on both fibres. This is also necessary as the ROD motherboard is expecting just one fibre per channel. For this purpose a new module, called PreROD or Optical Multiplexer Board (OMB) was conceived (Fig. 2). This board would be able to provide, in case of error in one link, the correct data to the ROD input by analyzing the CRC of the data packets on both fibers coming from the FEB.

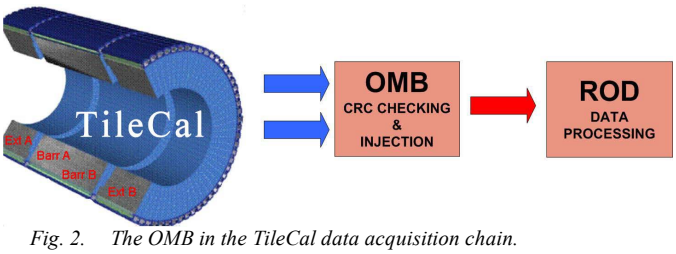

Fig. 2. The OMB in the TileCal data acquisition chain.

In the development of the work a new functionality for OMB was proposed. Because RODs should be tested in production stages and provided that in the first moments of LHC operation data may not always be available from front-end, it was suggested to include a "Data Injection Mode" to use the OMB as data pattern injector for ROD test and verification tasks.

The results of the first OMB 6U prototype are described in this paper as well as the functional description and technical specifications of the final OMB 9U prototype. Finally, the

Manuscript received November 4, 2007. (Write the date on which you submitted your paper for review.) This work was supported by the Spanish Committee for Science and Technology under Grant No. FPA2006-12672-C02-02.

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schedule for the OMB 9U production, installation and commissioning which will take place along this year is presented.

II. OMB 6U Prototype

The OMB 6U Prototype [5] was conceived as a first experience with the implementation of the functionality described above.

One of the operational modes is the checking the front-end data. This is based on the real time calculation of the CRC value of the data received on both input fibers. Once calculated, this value is compared to the one included within the data. If the values differ then the fiber is carrying defective data. Decision logic then selects which fiber will provide the data to the ROD motherboard, taking into account the results of the CRC checking.

The other OMB functionality is data injection to the RODs for tests and verification tasks. This function was used during the ROD production using the OMB 6U prototypes as data injectors to the RODs to verify the correct functionality of the ROD modules. These tests were also conducted to verify the behaviour of the OMBs.

A. Hardware description

The OMB 6U prototype (Fig. 3) has been designed as VME64x slave module architecture. It includes four optical inputs channels and two optical outputs, implemented with Infineon optical transceivers [7]. Both, the input and output links have a bandwidth of 640 Mbps (16bits@40MHz). There are also four input G-Link chips (Agilent HDMP-1034 [6]) on the board, two output G-Link chips (Agilent HDMP- 1032 [6]), two FPGAs for CRC calculations (CRC FPGAs) and one FPGA for VME interface (VME FPGA). These last are implemented in ALTERA devices [8]. Furthermore, for the data injector mode, the OMB has two additional copper input cables for trigger and busy signals.

Fig. 3. Picture of the OMB 6U prototype.

B. Functionality

There are two different functioning modes in the OMB: CRC processing mode and data injection mode. Fig. 4 shows the data distribution in the CRC mode. Two connectors receive the data and route them to the CRC-FPGA. Then, the CRC is checked and the decision is taken on which data is send to the ROD. Every time a CRC error is detected it is communicated to the VME-FPGA and the error counter is incremented. The values of these error counters can be read out in real time through the VME bus.

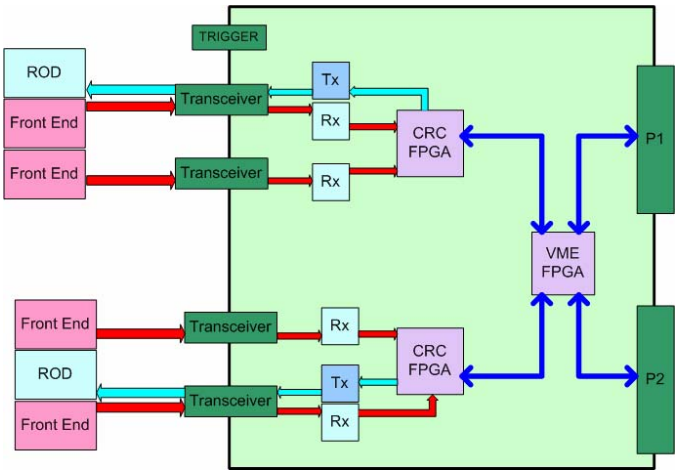

Fig. 4. Diagram of the OMB 6U dataflow.

In the data injection mode the optical receivers are not used and the input LEMO connector can be used to trigger the data injection. There are two different injection modes:

- Counter mode: The events have all words with the same value and this value is incremented with each event sent.
- Memory injection mode: The events sent are previously stored in the internal memory.

In both cases the events are sent every time a trigger is received in the CRC_FPGA either by the external LEMO connector in the front panel or by VME.

III. OMB 9U Final Prototype

The final OMB 9U prototype (Fig. 5) has been designed from the 6U board experience. This prototype is conceived in a 1 to 1 ratio with respect to RODs. This means that each final prototype will have 16 input links and 8 output links. Due to this modification a 9U format has been chosen for this new implementation.

With respect to functionality there are some minor modifications among which, the inclusion of the TTC receiver chip is the main one. This would lead to the possibility of triggering directly from the TTC system. In view of future upgrades and functionality the design includes four PMC connectors for mezzanine boards connected to the CRC FPGAs and is being designed for 80 MHz operating frequency instead of the nominal 40 MHz of LHC. This last issue poses some problems related to signal integrity and component placement aspects. Among them, the use of a single JTAG chain for the programming of all the FPGA chips in the board, the bus connecting the VME controller and the CRC controllers and the clock distribution are the main concerns.

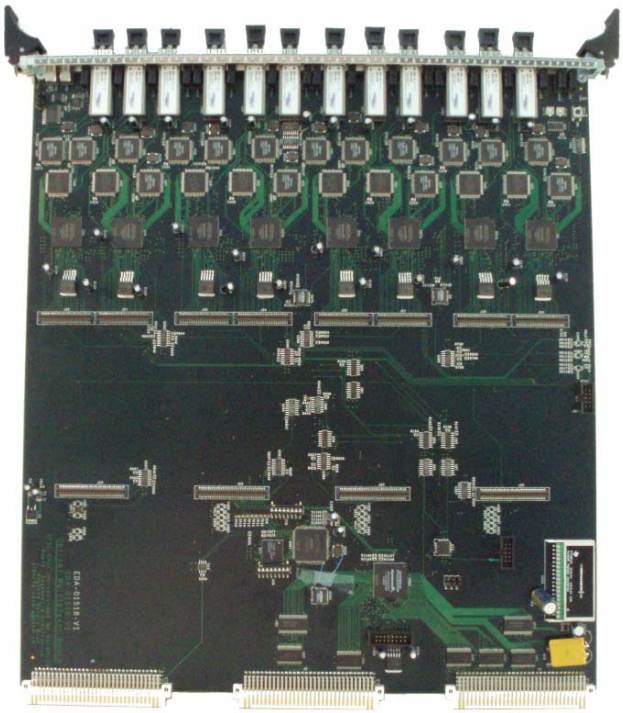

Fig. 5. Picture of the OMB 9U prototype board.

A. PCB specification

The OMB final prototype layout is a 10 layers PCB which optimize cross-section to minimize signal integrity problems. Fig. 7 shows the arrangement of layers. We tried to keep every signal layer between two power planes or, when it was not possible, routing the two adjacent layers orthogonally.

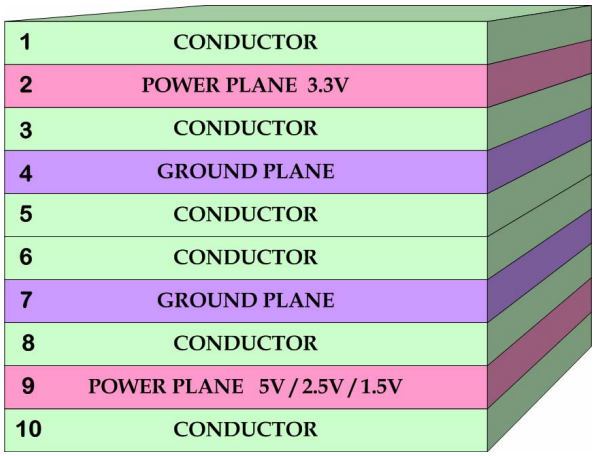

Fig. 6. OMB 9U prototype layer stackup.

Power distribution is also a concern in this board as we need several different supply voltages. For all the FPGAs we need 3.3 V for the I/O, while internal operation needs 1.5V. The NIM to TTL conversion for the external trigger signals needs a 12V supply voltage while other logic circuitry needs 5 V. The 12V and 5V power supplies are taken from VME bus or, when not available or for testing, from special pins on the board. Generation of the lower voltages (3.3 V and 1.5 V) is accomplish by DC voltage conversion from the 5 V main power supply. With this configuration, the power plane in layer number 2 was connected entirely to 3.3 V whereas the power plane in layer number 9 is a split plane with 1.5 V islands below the FPGAs (Fig. 7).

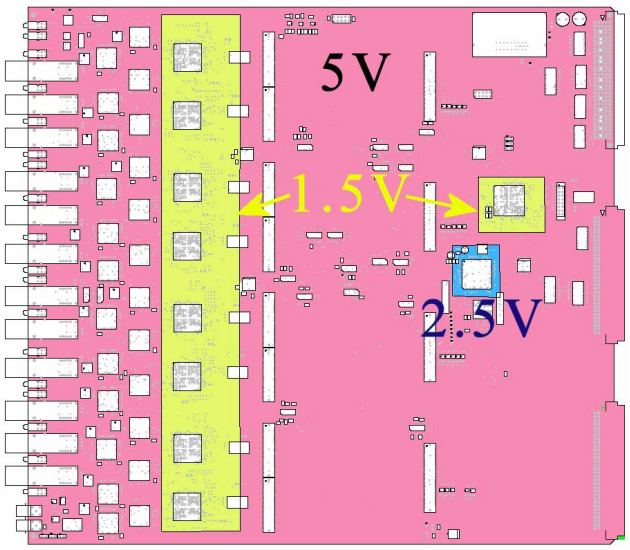

Fig. 7. Power distribution in the internal layer number 9.

B. Components

Fig. 8 shows the top assembly layer with the main components highlighted. In the OMB 9U board there are more than 1200 components connected with more than 2000 nets. Components are not uniformly distributed and they are mainly placed near the front-panel since these components are principally used to process or to inject data through the optical connector placed in the front-panel. The mezzanine connectors for daughterboard cards are mounted in the center of the board and the VME interface and the TTC receiver are placed close to the VME connector.

1) Optical Connectors

Stratos Lightwave dual optical receiver (M2R-25-4-1-TL) and transmitter (M2T-25-4-1-L) [10] have been chosen to optimize the space in the board. Since 16 inputs and 8 output links are needed there are 8 dual receivers and 4 dual transmitters in each board. The dual receiver connectors receive an optical fiber from front-end and transform it into a electrical PECL differential signal whereas the dual transmitter connectors transmit the differential signal to the optical fiber. These differential lines connecting the optical connectors and the G-Link chips were manually routed and with controlled impedance since these lines transmit high speed signals (640 Mbps).

2) G-Link chips

The G-Link chips are responsible of serializing (HDMP-1032) and de-serializing (HDMP-1034) [6] the data transmitted and received through the optical connectors. The HDMP-1034 receiver chip receives the differential signal directly from the optical receiver and transforms it into a 16-

bits bus. These chips are individually clocked with a 40 MHz oscillator placed close to the chip. On the other hand, the HDMP-1032 transmitter chip receives the 16-bits bus from the CRC-FPGA and transforms it into a PECL differential one. These chips are also clocked at 40 MHz but this clock is generated internally by the FPGA firmware. There are in total 16 receiver chips and 8 transmitters.

3) CRC-FPGA

The CRC-FPGA is the main component of the OMB 9U, since they are responsible of the data checking in the CRC operation mode and the generation of data in the injection mode. There are 8 CRC-FPGAs in each board and they are ALTERA EP1C12 devices [8], also used in the previous 6U prototype design. These devices will receive directly the front-end data for the CRC checking. Nevertheless, it will be possible to include more functionality, such as Bunch Crossing Identification (BCID) checking, since these devices will receive all the TTC information generated by the Central Trigger Processor (CTP) [11] through the TTCrx chip. All the error counters as well as the configuration and status registers are also included in the CRC-FPGAs firmware and they are readable and/or writable through the VME bus.

Besides, the CRC-FPGAs are connected to the Processing Units (PU) connectors allowing the system for future upgrade. In this case, the data received in the CRC-FPGA might be sent to the PU for processing tasks before its transmission to the RODs.

Finally, the firmware might be downloaded inside the CRC-FPGAs by using the JTAG chain or in a Passive Serial mode by using the Erasable Programmable Read-Only Memory (EPROM) memories mounted in the board. For this case, there are two EPROM for each 4 CRC-FPGAs.

4) VME Interface

The interface with the VME bus is managed by the VME-FPGA, which is implemented in a CYCLONE EP1C20 device. The VME-FPGA responds to VME geographical addressing and represents the interface between the VME bus and the CRC-FPGAs in order to read and/or write the registers physically placed in the CRC-FPGAs. It provides also the VME communication with the TTC-FPGA. Besides, the VME-FPGA might be used to internally generate a trigger signal in the injection mode.

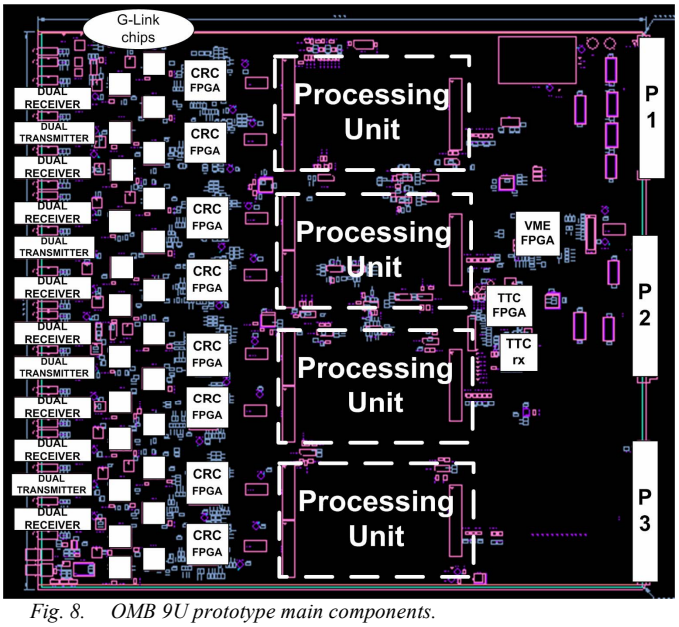

Fig. 8. OMB 9U prototype main components.

5) TTC Interface

The TTC [11] interface is implemented in the OMB 9U with a TTC receiver chip (TTCrx) and the TTC-FPGA. The TTC information is received in the TTCrx through the backplane and it includes the Bunch Crossing (40 MHz), the Bunch Crossing Reset (BCR), the Level 1 Accept (L1A), the Event Counter Reset (ECR) and the Trigger Type (TType). With these signals, the TTC-FPGA generates the Bunch Crossing Identification (BCID), the Event Identification (EVID). These signals and the TType are transmitted to each CRC-FPGA with each L1A received.

The TTC information might be used in the OMB 9U board to check the BCID of the data received from Front-End or inject data to the ROD with updated TTC information.

C. Operation Modes

1) CRC Checking

In the CRC checking operation mode the OMB 9U receives 16 fibers from 8 Optical Interface Boards (OIB) and transmits 8 fibers to one ROD (Fig. 9). Each CRC-FPGA has to check the CRC of two inputs and decide, in real time, which is transmitted to the ROD system. The decision algorithm is based on the storage of the events received through each input link in two different memories while the CRC is computed. The last word of the event includes the global CRC computed in Front-End over the entire event. When this word is received, the algorithm checks the CRC and decides which memory output is enabled.

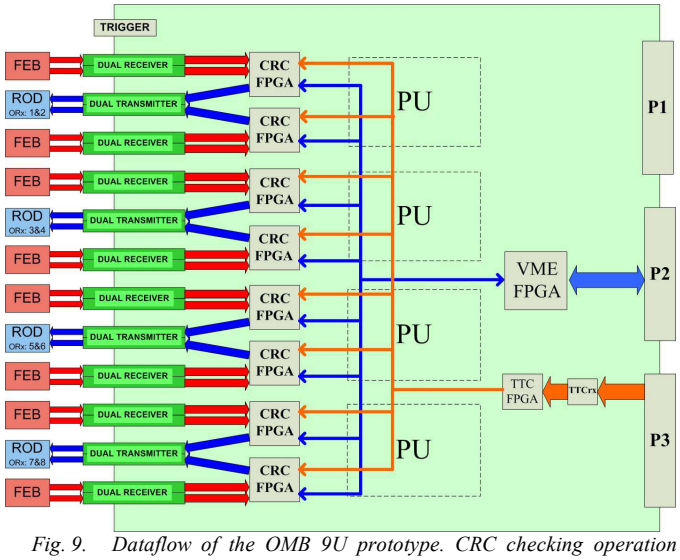

Fig. 9. Dataflow of the OMB 9U prototype. CRC checking operation mode.

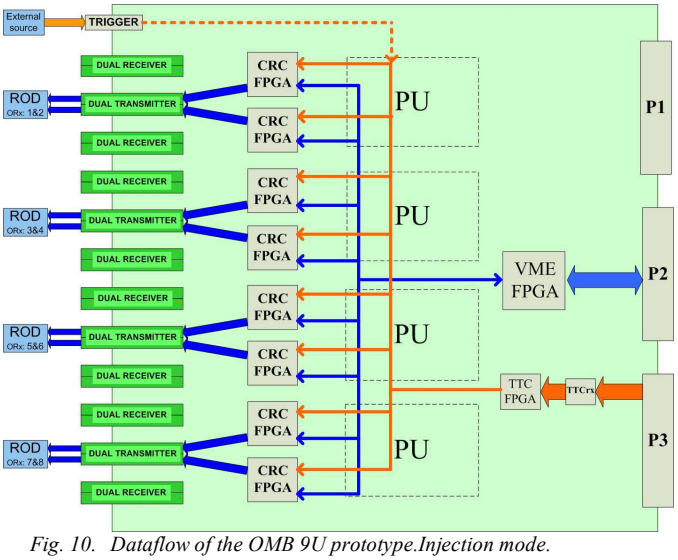

Fig. 10. Dataflow of the OMB 9U prototype.Injection mode.

In addition of the global CRC, it is possible to decide which fiber is transmitted to the ROD system by checking the DMU CRC included in the trailer of each DMU data (16 per event) or the BCID included in the header of each DMU data. All the errors detected are counted and stored in the corresponding internal register.

2) Injection Mode

There are two different injection modes as described above for the previous 6U board; the Counter and the memory injection modes. The main differences with the previous 6U version are the number of output channels and the possibility of injection of data with actual TTC information. With an OMB 9U it is possible to inject data to a whole ROD through its 8 optical outputs (Fig. 10). On the other hand, the TTC feature permits the injection of data with the TTC information received through the backplane. Since this information is also received at the ROD, it is possible to test the TTC synchronization at this level with the data generated in the OMB 9U.

3) PU Processing Mode

In addition, the OMB board can further process the data coming in with dedicated processing units (PU). This processing unit may be implemented using FPGA or DSP devices depending on the processing power needed. In particular, all the connections of the PU connector are fully compatible with TileCal ROD PU. With this mode, the OMB may perform some preliminary calculations prior to send data to ROD, allowing for a more powerful data processing in case it is needed. Fig. 11 shows the dataflow in the OMB for this operation mode.

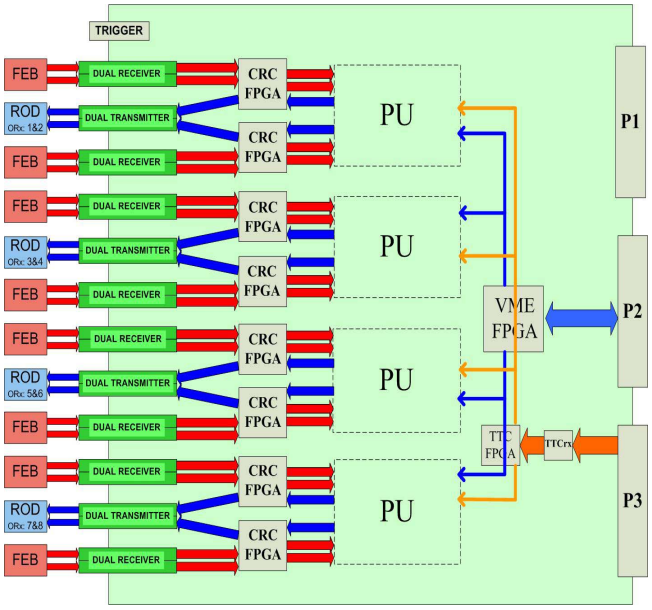

Fig. 11. Dataflow of the OMB 9U prototype. PU processing mode.

IV. OMB Firmware and Control Software

All the firmware for the FPGAs in the OMB board was designed using Altera Quartus II software. This software package also allowed us to perform the functional and timing simulations of the designs prior to download and test in the real device.

For the control software, Valencia group has already developped an application to control and run all the TileCal ROD crate for testing. This application is known as XTestROD. Within this application an special section (graphically displayed as a new tab window) was created to control the whole OMB board.

The OMB tab displays the information of the CRC error counters and the general status of the board. It allows also to set the control register bits that control the operational mode

of the board. Fig. 12 shows the XTestROD main window and the OMB tab displayed.

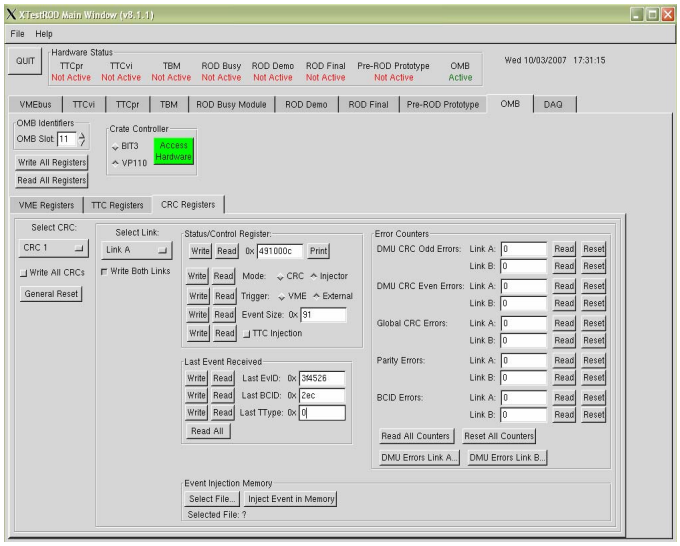

Fig. 12. XTestROD software and OMB tab.

V. Production Schedule

The first OMB 9U prototype board is actually being validated. The conclusions extracted during this phase will help us to carry out minor changes before starting the production. In the meantime, the firmware and control software are being completed to fulfill all the requirements.

The production will consist of 38 boards, 32 to be installed in the ATLAS cavern and 6 spares. The board production includes the fabrication, assembly and all the validation tests before its installation in the TileCal experiment acquisition chain. Fig. 13 shows the expected schedule for the production, installation and commissioning of the TileCal OMB 9U.

ID	Task Name	Start	Finish	Duration
1	Prototypes fabrication	12/02/2007	16/03/2007	5w
2	Software and firmware	01/02/2007	30/07/2007	25,6w
3	Prototypes validation	19/03/2007	02/07/2007	15,2w
4	Changes for the final version	03/07/2007	31/07/2007	4,2w
5	Production	01/08/2007	25/09/2007	8w
6	Installation and Commissioning	26/09/2007	05/11/2007	5,8w

Fig. 13. Schedule for the OMB 9U production.

VI. Conclusion

After a first prototype of the Optical Multiplexer Board in VME 6U format, a final 9U format board has been succesfully developed and tested. This board accomplishes with all the requirements specified by TileCal, so production phase is about to start. The board enhances the specification by adding new functionality (as the PU processing mode) and has been designed in view of the SLHC upgrade.

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