Installation and Commissioning of the TileCal Read-Out Drivers

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***Abstract*— TileCal is the hadronic tile calorimeter of the ATLAS experiment at LHC/CERN. The main component of the TileCal back-end electronics is the Read-Out Driver (ROD). The ROD system is placed between the first and the second level trigger and it is the responsible for processing the data gathered by the detector. The principal devices of the RODs are the Digital Signal Processors (DSPs) mounted in the Processing Units (PUs) daughterboards.**

The architecture and functionality of the RODs are briefly explained. Then, it is presented the ROD system installation in the ATLAS electronics cavern. Currently, the RODs are being used for the detector commissioning. It is detailed the Detector and Verification System (DVS) tests and TileCal calibration runs performed with RODs during the three commissioning phases.

***Index Terms*—Digital ignal processors, ATLAS, read-out driver, Optimal Filtering, DVS, commssioning.**

I. Introduction

TileCal is the hadronic tile calorimeter of the ATLAS experiment at LHC/CERN [1]. The main component of the TileCal back-end electronics is the Read-Out Driver (ROD) [2]. The ROD system is placed between the first and the second level trigger. The data produced in the detector are gathered and digitized in the front-end electronics and transmitted to the RODs through high-speed optical links. At the first level trigger rate the ROD system has to compute in real time information from 9856 front-end channels in less than 10 μs. Finally, the processed data are transmitted through optical links to the Read-Out System (ROS) located in the second level trigger.

II. Hardware System Overview

A. Back-End electronics system

The TileCal back-end hardware is placed between the first and second level trigger in the Data Acquisition (DAQ) chain (Fig. 1). It is divided in four Timing, Trigger and Control (TTC) partitions [3] corresponding to four detector partitions, two in the Long Barrel (LBA and LBC) and two Extended Barrels (EBA and EBC). Each TTC partition contains a ROD crate and a TTC crate. The ROD crate includes eight Optical Multiplexer Boards (OMB) for data checking and tests, eight RODs for data processing, eight Transition Modules (TM) for data transmission to the ROS system and a Trigger and Busy Module (TBM) [4] for busy generation.

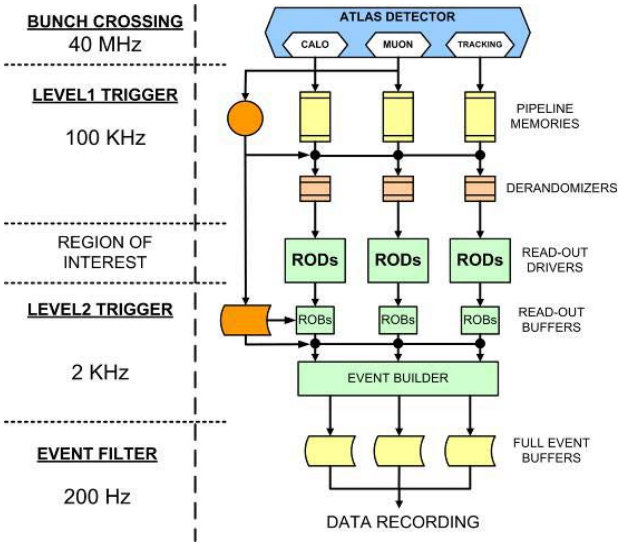

Fig. 1. ATLAS three level trigger architecture.

The TTC crate contains several TTC modules and it is the interface between each partition and the Central Trigger Processor (CTP).

B. TileCal Read-Out Driver

Each ROD receives the data from eight Front-End Boards (FEB) [5] through optical fiber links (Fig. 2). The input data is received in the ROD through 8 Optical Receivers and transmitted to 4 StagingFPGAs. The StagingFPGAs are the ROD input data distributor and transmit the received data to the Processing Units (PU) daughterboards. Two InputFPGAs receive, check and transmit the data in the PU towards two Digital Signal Processors (DSPs). The DSPs are the main component of the ROD since they are responsible for data reconstruction in real time at the ATLAS first level trigger rate

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[6]. The DSPs process and send the data to the ROD motherboard Output Controller FPGA (OCFPGA).

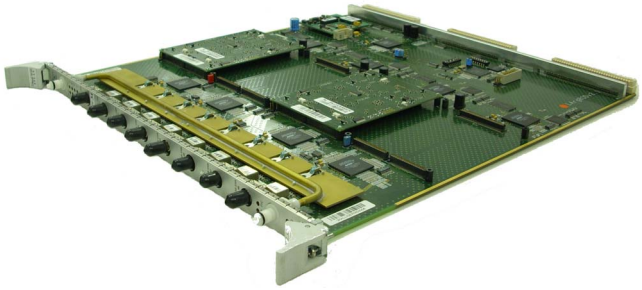

Fig. 2. TileCal Read-Out Driver.

Finally, the OCFPGA is the output data distributor and is responsible of data transmission to the Read-Out System (ROS) through the TM. Two more FPGAs provide the interface with the VME bus (VME&BusyFPGA) and with the TTC system (TTCFPGA).

III. TileCal ROD System Installation

The complete TileCal back-end electronics system is installed in three racks (Fig. 3) placed in the ATLAS electronics cavern (USA15).

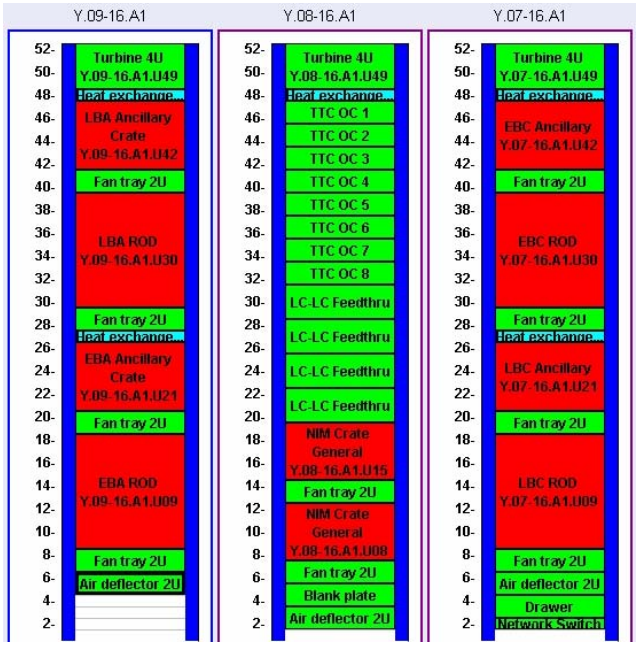

Fig. 3. TileCal back-end electronics racks distribution.

The four ROD and TTC crates are placed in racks Y.07 and Y.09. The A-side partitions (EBA and LBA) are placed in the Y.09 rack whereas the C-side partitions (EBC and LBC) in the Y.07 racks. These racks also include fan trays and air deflector for the electronics cooling.

The front-end data are received in the TileCal electronics cavern (USA15) in the patch panel rack Y.08 through optical fibers (Fig. 4). The optical fiber coming from front-end are plugged in the rear part of the patch panel. Since the OMB system is not yet available, during the commissioning phase the RODs are connected directly to the patch panel (Fig. 5). In the future, the OMBs will be connected to the patch panel and the RODs will receive the data from the OMBs.

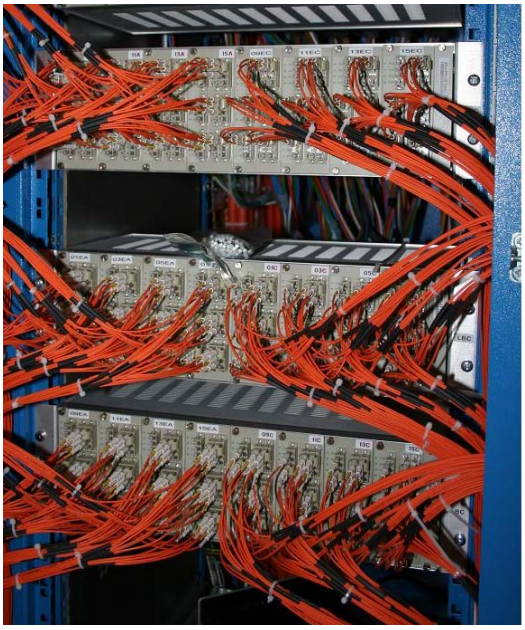

Fig. 4. USA15 optical fiber patch panel.

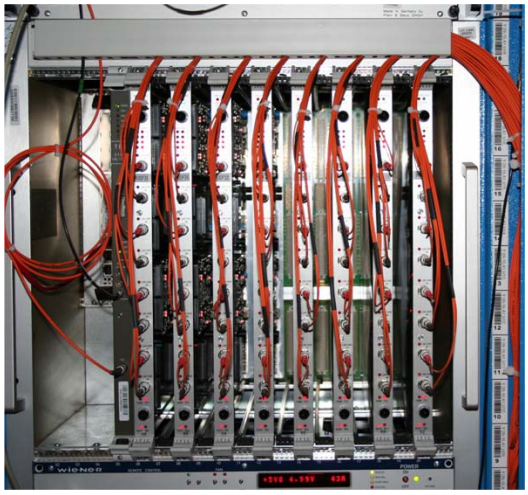

Fig. 5. ROD crate.

In ATLAS operation the TTC information is received from the Central Trigger Processor and distributed to front-end through the Optical Couplers (OC) (Fig. 6) [3]. During commissioning and stand-alone calibration tests the TTC information is generated in the Local Trigger Processor (LTP) placed in the TTC crate and distributed to front-end through the OCs.

The back-end electronics system has been installed simultaneously with the front-end drawers since both are necessary for the commissioning of the detector. The back-end installation started in summer 2005 and currently the system is completely installed.

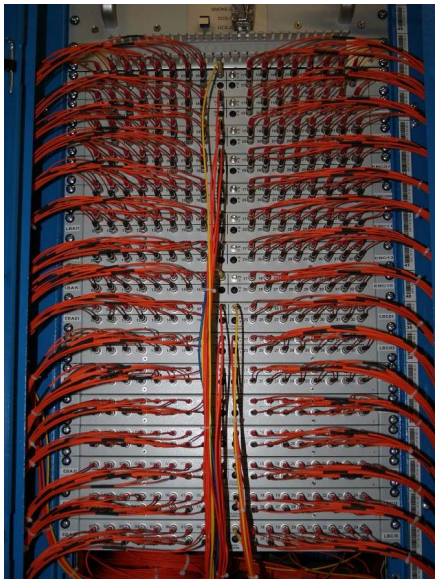

Fig. 6. TTC Optical Couplers rack.

IV. TileCal Commissioning

The TileCal commissioning is carried out in three overlapping phases. In the phase 1 the TileCal is commissioned in stand-alone mode. During phase 2 TileCal is integrated with other ATLAS sub-detectors (LAr, TRT, SCT and muon spectrometer) and with central DAQ, DCS and TTC. In phase 3 ATLAS is commissioned with cosmic runs. The TileCal RODs are being used for data taking in all the three commissioning phases.

A. Diagnostic and Verification System tests

Both front-end and back-end tests are needed for the commissioning of the TileCal detector. Complete certification cannot be achieved for the front-end if the back-end has not been completely certified and vice versa. Nevertheless, this deadlock can be avoided by certifying the back-end electronics without the front-end electronics. A full set of tests were performed at Valencia IFIC laboratory during ROD production in 2005 [7]**Error! Reference source not found.**. The ROD and TBM electronics underwent a two step validation procedure. First, a set of read write checks, refered to as register tests, plus a DSP processing unit test, followed by a bit transmission and CRC check to assure a 10^9 bit error rate.

The front-end digital read-out DVS tests are a set of tests that intend to detect problems prior to the data acquisition [8]. The tests measure the detectors response against a charge injection on the 3in1 cards of the super-drawer. The check will be done for the two ranges High Gain and Low Gain, referred to in the text as CIS HG and CIS LG. Another type of test will check the pedestal level at high and low speed.

In the CIS tests a trigger application sends 100 CIS signals and 100 triggers to the super-drawer. The read-out application reads out 100 events from the super-drawer in calibration mode (7 samples 2 gains).

Once the data is read-out into the memory of the ROD crate controller, it is analyzed. The global CRC, the Bunch Crossing Identification (BCID) of every event and the fragment ID of the header is checked over all events.

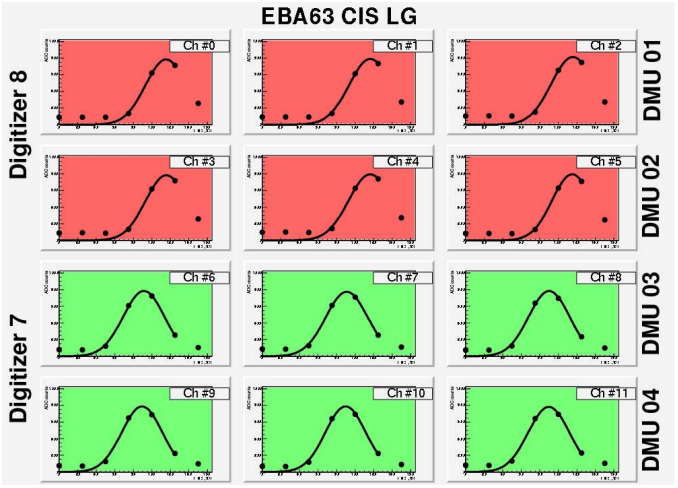

Fig. 7. Plot of a CIS tests result.

As a part of the specific analysis of the data for CIS, the CIS pulse shape is checked [9]. The raw samples are fitted to a Gaussian function which is not very accurate. The amplitude and the width of the pulse are compared to the expected values. If only one of the pulse shapes is wrong, the corresponding plot will be painted red and the file tagged as bad (Fig. 7).

The first event is printed into a post script file containing two sheets with one canvas with 24 plots each. As the long barrel super-drawers have 45 PMT blocks populated, only 45 plots in the post script file are filled. Accordingly, the extended barrel post script result files contain 32 plots. The numbering goes from 0 to 47 where 0 corresponds to the inner most PMT.

In the pedestal test a trigger application sends 100 triggers to the super-drawer. The read-out application reads out 100 events from the super-drawer in calibration mode (7 samples 2 gains).

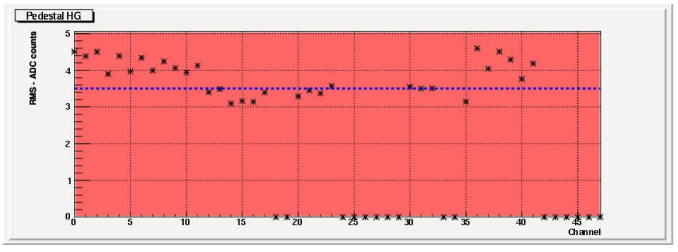

Fig. 8. Result of a pedestal test of a noisy channel.

Once the data is read-out into the memory of the ROD crate controller, it is analyzed. The global CRC, the BCID of every event and the fragment ID of the header is checked over all events.

The noise in both high and low gain is computed. If the noise of one PMT is higher than the threshold, 1.5 ADC count in low gain and 2.5 ADC count in high gain, the test is failed. The result is a post script file with one sheet divided into two canvases, one for the high gain and one for the low gain. If the test fails, the canvas is painted red (Fig. 8) whereas if the test is OK, the canvas is painted green (Fig. 9).

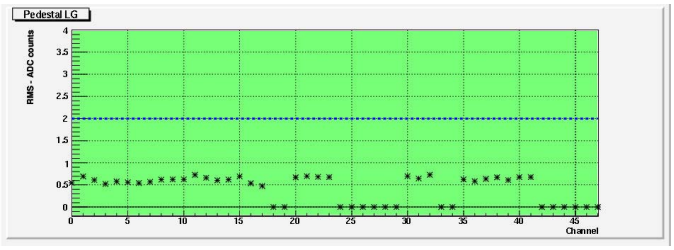

Fig. 9. Result of a pedestal test of a good channel.

B. *TDAQ commissioning runs*

The ATLAS Trigger and DAQ (TDAQ) software controls the data flow and acquisition for the TileCal commissioning data taking (Fig. 10) [10]. The TDAQ configuration for phase 1 is in stand-alone mode for calibration runs (CIS, pedestal, laser), and for phase 2, integrated with other sub-detectors for physic runs with cosmic trigger. The raw data are read-out and online processed with Optimal Filtering and Level 2 algorithms in the RODs [11.

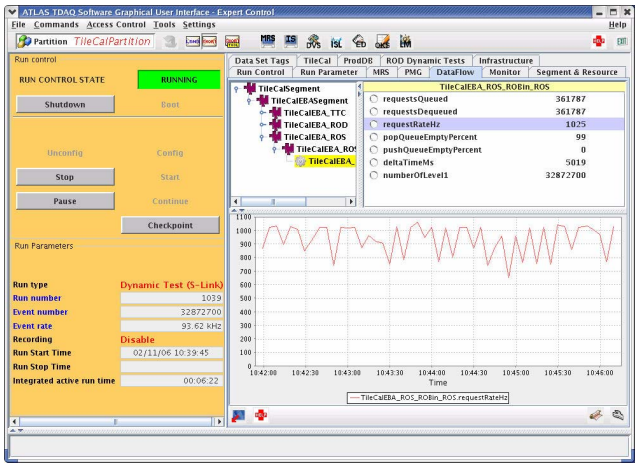

Fig. 10. TDAQ software snapshot.

After the data acquisition the byte-stream is offline analyzed to certificate the detector. It is important to perform some validation on the data prior to physics analysis. This is done through the TileCal standalone offline framework. It includes the storage of the data in CASTOR, reconstruction of the data in multiple n-tuple files (one per super-drawer module) and a set of data quality checks which are performed automatically over the data.

The CRC and BCID check is performed on all types of runs. A plot shows the result of CRC check as a function of the digitizer number from 0 to 15. It is also implemented a stuck bits and zero amplitude tests looking the amplitude distribution in ADC counts.

In addition some other performance tests are also implemented to check the amplitude over the charge injected ratio and the time over the CIS phase. The mean amplitude and RMS and the mean time and RMS are especially important for LED and CIS runs to monitor the stability of electronic response to a signal. In LED runs it is also checked the stability of the phototube response.

In pedestal runs it is checked the RMS of the pedestal distribution to find noise channels as well as the correlation and covariance of the amplitude to find a source of coherent noise.

V. Conclusions

The TileCal ROD system is completely installed in the ATLAS electronics cavern. The ROD system is being used for DVS tests and data acquisition for front-end modules certification within the TileCal commissioning phase 1. Furthermore, in commissioning phase 2 the RODs have been integrated within the rest of ATLAS sub-detectors and within the ATLAS central systems. In the commissioning phase 3 the RODs are participating in physics runs with cosmic rays using a setup of ATLAS close to operation.

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