The Optical Multiplexer Board for the ATLAS Hadronic Tile Calorimeter

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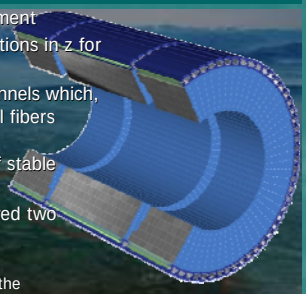
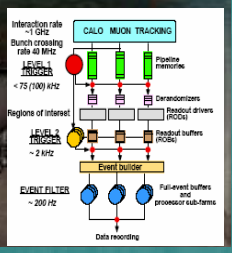
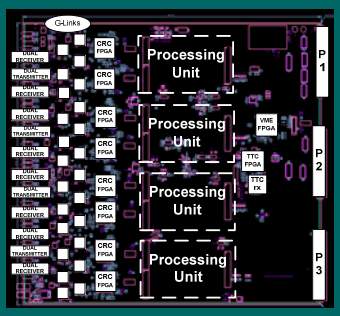
Framework

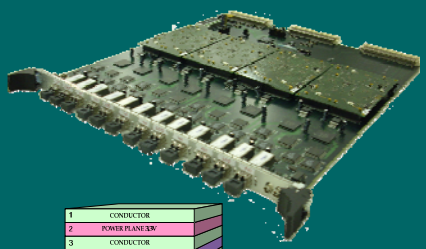
- TileCal is the hadronic calorimeter of the ATLAS experiment
- TileCal detector is divided in 64 modules in ϕ and 3 sections in z for a total of 256 modules
- The read-out is carried out using 10.000 electronic channels which, after digitization, come out of the detector using optical fibers towards the Read Out Driver (ROD) module
- ATLAS requires radiation tolerant electronics capable of stable operation for, at least, 10 years
- Radiation tests of the front-end digital electronics showed two kind of non destructive errors prone to happen:
  - Transient error in the data flow
  - Permanent error in the data flow which require the reset of the electronics
- The solution adopted was to add two ADC and two control FPGAs provide fault tolerance two optical fibers per channel with redundant information
- A modification in the readout architecture was conceived to include a module which would check data consistency in both fibers and select the error free one to pass to ROD module
- This module is the Optical Multiplexer Board (a.k.a. PreROD module)

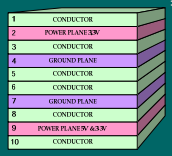




Optical Multiplexer Board 9U Final Design



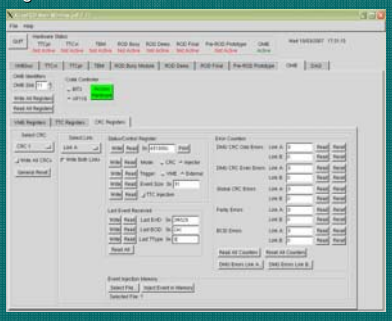




- 2nd prototype validated. Some minor changes with respect the first one
- 1 to 1 ratio with RODs
  - 16 Front-End inputs.
  - 8 output to ROD
- Board fully operational. No more changes for production.
- Ready for the SLHC
  - Designed to work at 80 MHz input data rate
  - Processing Units slots for data reconstruction
  - Optical outputs for the read-out
- 4 Processing Units
- Compatible with ROD PUs
- Pre-processing of front end data
- Cadence Allegro and SI Explore CAD used in design

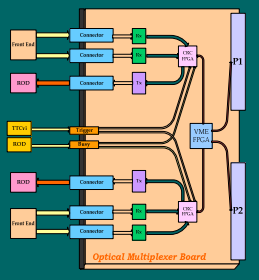
OMB Firmware and Control Software

- Altera Quartus II used in FPGA firmware design and simulation
- OMB panel in the XTestROD software
  - Global CRC checking and decision
  - Registers with error counters
- Injection mode
  - Auto generated events
    - With global CRC
  - With real TTC information
    - DMU data blocks structure (samples & gains)
- CRC errors generation
- Internal memory injection
  - Real data files



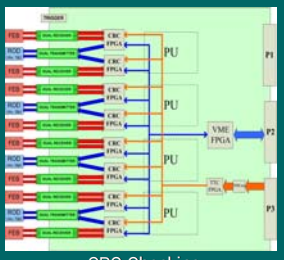
OMB First Prototype Hardware Design

- Specifications
  - VME 6U Board format
  - 2 input channels (4 input fibers) @ 640 Mbit/s
  - 2 output channel (2 output fibers)
  - Digital data analysis (CRC computation)
  - Trigger and Busy inputs
- Functionality
  - Error detection (multiplexing)
  - Data injection
    - Preconfigured event (counter)
    - Configurable event loadable through VME
  - Different trigger options
    - External
    - Internal. Variable frequency
      - Single
      - Loop
      - Non-stop
- First prototype finished in June 2004
  - Validate OMB functionality
  - Validate PCB design and signal integrity practices
  - Used in ROD production tests
    - Injection of data (fake and real from TB)
      - ROD functioning
      - DSP algorithms

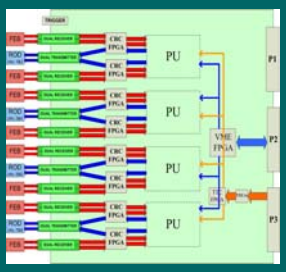


OMB Final Design Functionality

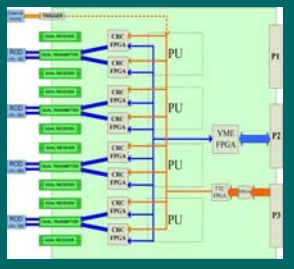
- Real time CRC checking
  - GLOBAL
  - DMU CRC
- TTC Information
  - BCID DMU check
- Error counters readable from VME
- Data injector to RODs
  - Actual data
  - Autogenerated data
- Trigger
  - External source
  - TTC information



- CRC Checking



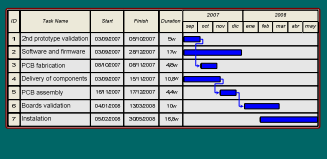
- PU Processing



- Data Injection

Production Schedule

- Production of 38 boards.
  - PCB fabrication in Barcelona (2 weeks)
  - Assembly in Valencia (1 month)
- Stock up of components
- ROD production test-bench used for the validation of the boards
  - 4 boards tested per week
- OMB system fully installed spring '08



Conclusion and future work

- After first OMB prototype success now we have an ATLAS OMB design ready for production
- Test of this final prototype were successful
- Now starting component procurement for production
- Expecting to have the OMB system installed by spring 08

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