

Real Time Data Acquisition with Read Out Driver System

J. Torres, V. González, J. Soret, E. Sanchis, J. Martos, J. A. Gómez
 Dept. Ingeniería Electrónica, Universidad de Valencia – ETSE

J. Castelo, C. Cuenca, A. Ferrer, E. Fullana, E. Higón, J. Poveda, B. Salvachúa, C. Solans, J. A. Valls
 I.F.I.C. – Centro Mixto Universidad de Valencia – C.S.I.C.

Abstract--The Read Out Driver (ROD) system is a real time data acquisition system for the TileCal calorimeter included in ATLAS detector for Large Hadron Collider (LHC) experiment. This experiment is the most important particle accelerator that is being constructed at CERN (European Laboratory for Particle Physics).

This new generation of detectors requires highly hardened electronics, able to deal with a huge amount of data in real time. The data chain from First Level of Acquisition to a Second Level of Acquisition is closed, through the ROD, with optical links.

Some on-line data processing is done in the Programmable Logic Devices (FPGAs) and Digital Signal Processors (DSPs) where different algorithms are implemented. Preliminary offline analysis show promising results.

This paper describes the status of the ROD, its evolution and the Test Beam Set-Up realized in Super Proton Synchrotron beam at CERN.

I. INTRODUCTION

THE CERN (European Laboratory for Particle Physics) in Geneva is working in new particle physics research. To develop this research, a new accelerator, the *Large Hadron Collider (LHC)* is presently being constructed. In the year 2007 beams of protons are expected to collide at a center of mass energy of 14 TeV. In parallel to the accelerator, two general purpose detectors, *ATLAS (A Toroidal LHC Apparatus)* and *CMS (Compact Muon Solenoid)*, are being developed to investigate proton-proton collisions in the new energy domain and to study fundamental questions of particle physics.

Each detector is composed of several subdetectors, TileCal is one of these. They are prepared to read, in each collision, through thousands of electronic channels a high data volume. Therefore, to make the integrated analysis of all their information its necessary new real time systems. The work we present here is included in the studies and development currently carried out at the University of Valencia and IFIC for the Read Out Module (ROD) of the hadronic calorimeter TileCal of ATLAS.

II. TILECAL ROD SYSTEM

TileCal is the hadronic calorimeter of the ATLAS experiments. It consists, electronically speaking, of 10000 channel to be read each 25 ns. Data gathered from these channels are digitized and transmitted to the data acquisition system (DAQ) following the assertions of a three level trigger system [1].

In the acquisition chain, place is left for a module which has to perform preprocessing and gathering on data coming out after a good first level trigger before sending them to the second level. This module is called the Read Out Driver (ROD). Figure 1 shows this structure schematically.

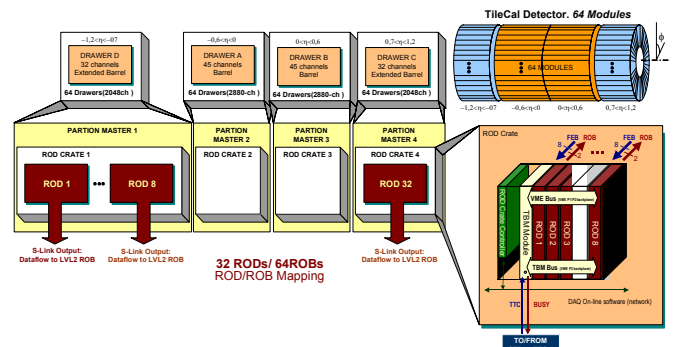


Fig. 1. TileCal ROD System.

For TileCal, the ROD system will be built most probably around custom VME boards which will have to treat around 2 Gbytes/s of data. Intelligence will be provided to do some preprocessing on data.

For the reading of the channels we are working on a baseline of 32 ROD modules. Each one will process more than 300 channels. The studies currently going on at Valencia focus on the adaptation of the first prototype for TileCal needs.

The basic schema to use is based on the ROD crate concept in which ROD modules are grouped into VME crates jointly with a Trigger and Busy Module (TBM) and possibly other custom cards when needed. This ROD crate interfaces with the TileCal Run Control and the ATLAS DAQ Run control.

The basic functions and requirements of all ATLAS ROD can be summarize saying that the ROD board receives the data from the Front End Boards [2] which after some processing are sent to the next level of process, Read Out Buffers (ROBs). These data may be buffered to be able to work with the maximum Level 1 trigger rate (100 KHz) without introducing extra dead time.

For each particular detector, some preprocessing could be done at ROD level. For TileCal, RODs will calculate energy and time for each cell using optimal filtering algorithms besides evaluating a quality flag for the pulse shape (χ^2). RODs will also do the data monitoring during physics runs and make a first pass in the analysis of the calibration data leaving the complete analysis to the local CPU of the ROD crate.

In some cases data will not be processed and will flow raw to Level 2. These include interesting events, large energy depositions in a cell or debugging stages.

It will be also desirable to have the functionality to apply corrections to the energy or time estimators for example to correct the non-linearities in the shaper or in the ADC.

Finally ROD will monitor the Minimum Bias and pile-up noise and will have the possibility of working in special runs at reduced trigger rate.

III. ROD MODULE

The ROD motherboard (figure 2) is a 9U VME64x board, which holds in its core four PUs mounted as mezzanine boards (120x85 mm). These mezzanine are composed of two DSP blocks each, able to treat up to 128 channels (LiAr RODs) or up to 45 channels (TileCal RODs) operating in normal mode. Each DSP block is composed of an input FPGA, a TMS320C6414@600 MHz DSP from Texas Instruments and an output FIFO.

The mezzanine also contains an output FPGA used for the VME and TTC interface of the ROD [3]. The current choice of DSP provides sufficient flexibility to choose between different schemes in data processing.

The main functionalities of the PUs can be summarized as:

- Dataflow management, data formatting, TTC (trigger) reception, buffering and synchronization.
- Data processing with reconstruction algorithms.
- Error detection.

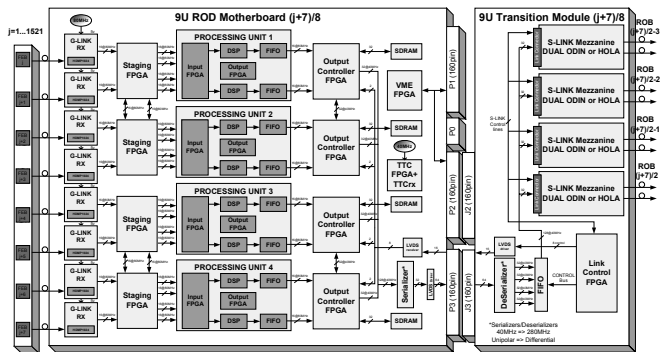


Fig. 2. ROD Motherboard.

The main description for the ROD is:

A. Input Bandwidth

The maximum input BW of each link for a TileCal physic event is 467.2 Mbit/sec, so 4 links (4 drawers) is 1.825 Gbits/sec. Input bandwidth of the Processing Unit is 2,5 Gbits/sec (64bits@40Mhz) => One PU has enough input BW for 4 links.

B. The Processing Unit

We need to process 154 channels (four drawers) in two TMS320C6414@600MHz DSPs (4800 MIPS each). This DSP has the same core with some improvements in number of registers and an enhanced DMA unit over the actual DSP we have tested is the TMS320C6202@250MHz (2000 MIPS). Our actual lab routines could process 45 channels in around 5.5 ms (assembler) or 15.5 ms (C code).

C. Output Bandwidth

The typical BW for 154 channels (four drawers) is 656 Mbits/sec. Then, an Output Controller FPGA of 1.28 Gbits/sec (32@40MHz) has enough BW for the output of each Processing Unit (154 channels each).

The ROD has a double optical receiver and two 3.3 V HDMP1034 RX chips with 40 MHz clock for data de-serialization and staging FPGA machine clock. A FIFO for at least two input events is suggested because we need a temporary storage for the redundancy link data, while we are checking the CRC for one of them, in case of errors we read from the FIFO the other unit link fragment and we use this one if it's OK. If not an error flag must be reported.

There will be a total of 32 ROD VME64x boards to read the whole TileCal detector, with up to four PUs (Processing Units) each.

A basic list of the ROD functionalities include:

- To receive, process and check data consistency from the FEBs (Front-End Buffers) through eight optical fibers.
- To calculate energy and time through an optimal filtering method at the PU DSP (Data Signal Processor) level. The result is sent to the ROB (Read-Out Buffer) modules where this information is made available for subsequent trigger decisions.
- To monitor the data to ensure a good quality data logging.
- To generate BUSY signals to the CTP (Central Trigger Processor) in case of problems in the data treatment by the DSPs

The RODs operate an optical-to-electrical conversion through optical receivers and ensure full compatibility with the FEB output data format.

Due to the reduced channel density of the TileCal with respect to the LiAr calorimeters, the TileCal RODs can operate with 50% of the PUs and S-Link outputs (the RODs support up to four S-Link output mezzanine cards called Link Source Cards).

IV. OPTICAL MULTIPLEXER BOARD

TileCal is a redundant data acquisition system. Two optical fibers carry the same data from front-end electronics to ROD. This is necessary because of radiation phenomena could cause malfunctions inside front-end electronics, and bit and burst errors over data ready to be transmitted to ROD card. Unfortunately, ROD card has only one input connector for each data, because the original design responds to initial specifications.

Our primary target is to improve error tolerance, designing a pre-ROD card, called Optical Multiplexed Board (OMB), able to analyze two fibers, both of them carrying the same data, to provide the correct one to the ROD input.

The interest of this project was justified in February 2003, when a preliminary study appeared. This proposal shown a solution for OMB based on exhaustive on-line analysis of the data carried by both of the fibers, using FPGAs for implementation. This architecture was called as "MiniROD", because it follows a ROD-like design.

Universidad de Valencia – IFIC (Spain) team showed the greater interest to deal with this project, to make a first prototype to study technical viability. In particular, the main goals are:

- Fiberoptic switching to take advantage of redundancy.
- Obtain real (production) costs.
- Have a development platform (hw - sw).
- Try different alternatives for data error analysis (CRC, etc.).

A new functionality for OMB was proposed, it was suggested a function mode called "Data Injector Mode", to use the OMB like data pattern injector towards ROD for test and verification uses

This project started in October 2003. The construction of an OMB first prototype is finished.

Optical Multiplexer Board prototype has been designed to readout redundant output data from FEBs [4] and send correct data to RODs. The mother board prototype is a 6U VME64x slave module which has two channels. In addition, it works like ROD Injector in order to test ROD Motherboard.

The layout of the board is shown in Figure 3.

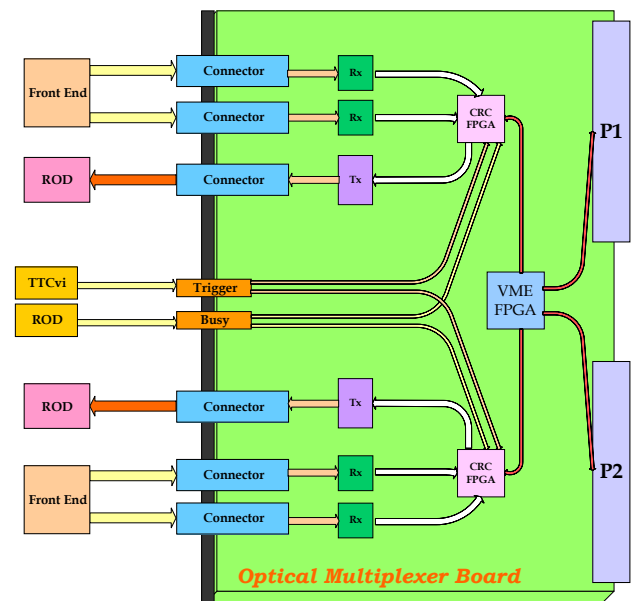


Fig. 3. Optical Multiplexer Board Block Diagram.

The Optical Multiplexer Board includes four optical inputs connectors and two optical outputs connectors integrated in the PCB. The input channels are capable of reading 4x16 bits at 40 MHz and allow us to test different input technologies. The output will also run at 40 MHz with a data width of 16 bits.

On the board there are also four input G-Link chips, two output G-Link chips, two CRC FPGAs and one VME FPGA. These last are implemented on ALTERA devices. Furthermore, for Data Injector Mode, OMB has two more inputs. Trigger and Busy external signals are included in this prototype to send correctly internal data in order to test ROD functionality [5].

A short description of the main functions of the G-link and FPGA chips in the OMB board is given in Table 1.

TABLE I
OMB PRINCIPAL COMPONENTS

Component	Main Function	Chip
6 G-Link Chips	Deserialize the incoming data. Serialize the output data.	HDMP-1034 HDMP-1032
2 CRC FPGAs	Send correct data to ROD. ROD Injector Data.	CYCLONE EP1C12
1 VME FPGA	Interfaces OMB to VME.	ACEX EP1K100

V. DATA ANALYSIS

A final check of the ROD motherboard functionality consists in the comparison of the output from the on-line processing on DSP and the off-line analysis of raw data [6]. The offline analysis was performed with C++ libraries on ROOT environment.

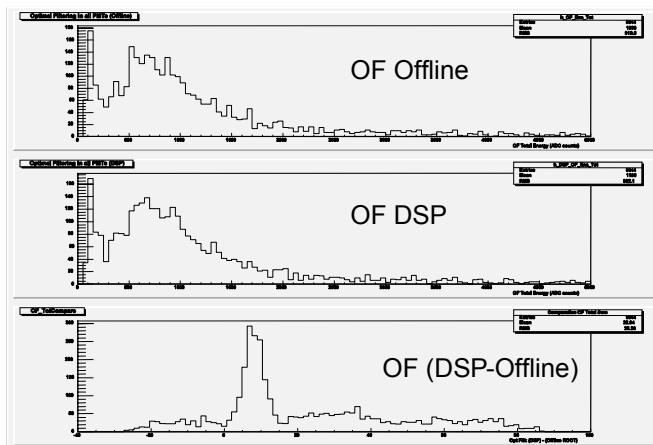


Fig. 4. Optimal Filtering Energy Reconstruction.

Data was taken in the late August 2003 run. Two algorithms were applied: Optimal Filtering and Flat Filtering [7]. Histograms of the difference of the results of the on-line and off-line calculations for photomultiplier number 16 of the positive side of the central barrel are shown in figures 4, 5.

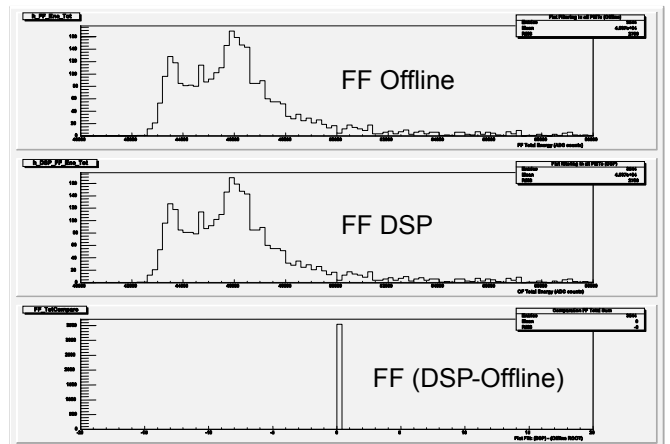


Fig. 5. Flat Filtering Energy Reconstruction.

A. Optimal Filtering

Optimal Filtering is a more sophisticated method. It requires a careful implementation in the DSP because it uses coefficients for scaling the different samples. The implementation of this algorithm involves sensitive operations like truncation and rounding up. As it is seen in figure 4, differences appear between on-line and off-line calculation, mainly due to the usage of different kinds of variables and operators. Even so, those differences are below 2 ADC.

B. Flat Filtering

This algorithm sums all nine raw data samples of one event. It is a simple algorithm to implement in the DSP and very quick to compute. The top histogram in figure 5 shows that there are no differences in the on-line and off-line reconstruction.

VI. REFERENCES

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