Setup, Tests and Results for the ATLAS TileCal Read Out Driver Production

J. Castelo[a], V. Castillo[a], C. Cuenca[a], A. Ferrer[a], E. Fullana[a], V. González[b], E. Higon[a], A. Munar[a], J.Poveda[a], A. Ruiz-Martínez[a], B. Salvachua[a], E. Sanchís[b], C. Solans[a], J. Soret[b], J. Torres[b], A. Valero[a], J. A. Valls[a]

[a] Departamento de Física Atómica, Molecular y Nuclear and IFIC, Aptdo. 22085, Valencia, España
[b] Departamento de Electrónica, Universidad de Valencia, España

Alberto.Valero@ific.uv.es

Abstract

In this paper we describe the performance and test results of the production of the 38 ATLAS TileCal Read Out Drivers (RODs). We first describe the basic hardware specifications and firmware functionality of the modules, the test-bench setup used for production and the test procedure to qualify the boards. We then finally show and discuss the performance results.

I. INTRODUCTION

The back-end hardware for the first level trigger and DAQ of the ATLAS Hadronic Tile Calorimeter (TileCal) consist of four ROD crates. Each ROD crate contains eight RODs and eight Transition Modules (TM) and reads out one out of four partitions in the calorimeter [1]. Therefore, 32 RODs and 32 TMs are needed in order to read out the whole calorimeter. Taking into account the spare units, we have produced and tested a total amount of 38 units of RODs and TMs.

A. The TileCal ROD module

Both the electromagnetic and hadronic calorimeters in ATLAS use a common ROD motherboard (Figure 1) adapted to the specifications required in each case [1]. For this reason, the motherboards were produced together.

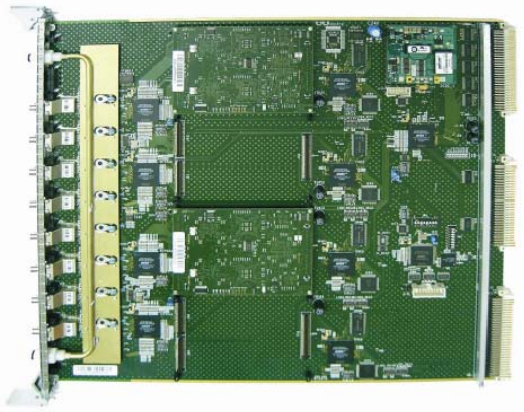

Figure 1: ROD motherboard with 2 Processing Units.

At industry level some general, mechanical checks, JTAG boundary scan and X-ray tests were done for all the RODs. Besides, at the University of Geneva (UniGe) some static tests were done to all the RODs by the Liquid Argon (LAr) group in order to verify the correct functionality of all the components in the board. In addition, several dynamic tests to check the dataflow across the ROD were also done at UniGe [2].

Once the RODs were delivered to the TileCal group, the first task was to adapt the boards to the TileCal requirements before their validation tests. This adaptation consists of some hardware modifications and firmware changes [1]. The hardware modifications customize the ROD to receive the data at the working frequency of the Front End (FE) Interface Cards. Furthermore, the number of Processing Units (PUs) per ROD has to be adapted also, due to the fact that TileCal will use 2 PUs per ROD (called Staging mode), instead of 4 PU/ROD used in the electromagnetic calorimeter of ATLAS (full mode) [1].

Concerning the firmware, specific code for the TileCal ROD in the StagingFPGA, InputFPGA and DSPs is used [1]. As the InputFPGA and DSP code is downloaded at configuration time, only the StagingFPGA code has to be downloaded before the beginning of the tests. Besides, if some code is upgraded for specific or common firmware, it has to be checked and validated prior to be updated in all the boards.

Regarding the TMs, the difference between both calorimeters is the number of High-speed Optical Link for ATLAS (HOLA) mezzanine cards mounted on the boards. LAr ROD system implements four HOLAs per TM, whereas TileCal system uses two HOLAs per TM [1].

II. TEST-BENCH DESCRIPTION

The test-bench mounted in the lab at IFIC-Valencia for the TileCal RODs validation was divided into an injection part, a ROD crate and an acquisition system (Figure 2).

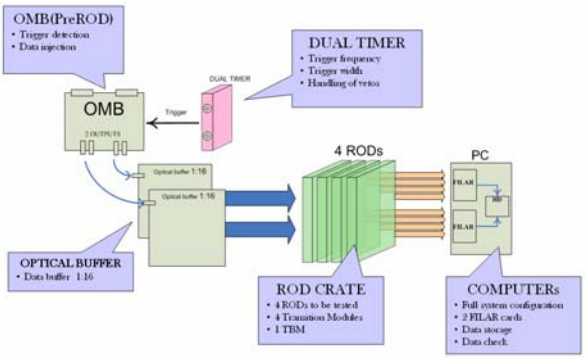

Figure 2: Test-bench diagram.

The FE was emulated by injecting data to the ROD with one Optical Multiplexer Board (OMB) 6U prototype, two Optical Buffers and a dual timer to control the rate of injection.

Up to four RODs in a crate could receive and process data simultaneously and a PC system equipped with 2 FILAR cards gathered, stored and checked all the data coming from the RODs.

Furthermore, one more computer was included in the setup as the main user interface computer responsible for the configuration tasks of all the devices in the test-bench chain.

B. Optical Multiplexer Board prototype

Preliminary studies done on the FE electronics showed that radiation shouldn't be a problem at the beginning of the experiment. Nevertheless, these studies also showed that radiation could cause malfunction, bit errors and durst in the data sent, in particular when the luminosity of the beam will be increased.

In order to avoid these radiation problems, each drawer in the FE will send data to RODs redundantly by two different optical fibers. The final OMB should check the CRC and decide in real time which data is correct and send it to the ROD.

The OMB integrated into the RODs production test-bench was a 6U VME prototype version of the final 9U VME OMB (Figure 3). It has four optical inputs and two optical outputs. Two CRC_FPGAs are mounted and connected, each of them, with two inputs and one output, and they are responsible of CRC check and injection tasks. In addition, a VME_FPGA provides communication between the VME bus and the CRC_FPGAs. The interface with VME is used for configuration tasks and readout CRC error counters [3].

Apart of the CRC check in real time, the OMB was designed to emulate the FE in order to have the possibility to perform ROD calibration and tests while the detector is not working. For these purposes, the OMB can inject events to the ROD in two different modes. These two options were used during the production of the RODs. In the first one, the events have all the words equal, but events are always different between them. In the second mode, the OMB was capable of sending a user defined event, downloaded in advance, even with real data, and it sent the event to the ROD with every trigger signal. Both, the configuration of the injection mode and the event download are done by the VME bus.

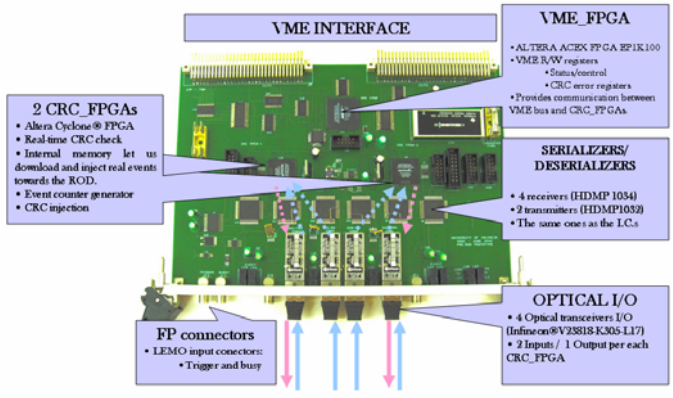

Figure 3: Optical Multiplexer Board 6U prototype.

The counter mode was used in long term runs in order to inject a high quantity of different events at high rate, while memory events, which have to be downloaded before its injection, can not be used at high rate if different events are needed. Nevertheless, this memory mode was used in order to validate the DSP reconstruction code, due to the possibility of inject events with real data.

As part of the raw data format every event sent by the OMB includes in the last word (apart of control words) the CRC calculation of the whole event. This CRC word can be checked after the acquisition chain in order to prove the correct dataflow across the system.

Apart of the injection modes, the trigger has also two modes: external and internal. In the external mode, the trigger signal has to be provided and generated in a dual timer, where the rate of injection and the width of the pulse are configured. On the other hand, if internal mode is selected, the rate of the trigger is configured in the OMB.

C. Optical Buffer 1:16

The Optical Buffer (OB) is a 9U VME board specifically designed for ROD production (Figure 4). As the OMB 6U prototype offers only two optical outputs and the ROD has 8 inputs, the OB was designed in order to increase the number of links injecting data to the RODs. The OB receives one optical input, converts the signal into LVPECL, and repeats it to 16 optical outputs with clock drivers.

With only one OMB 6U prototype and 2 OBs we had 32 links, which is enough to inject data to 4 RODs at the same time. It represents a half partition of the TileCal detector.

Figure 4: Optical Buffer 1:16.

In counter mode, the OMB was programmed to inject different events through each output. The two outputs were repeated with two OBs. Note that to inject only two kinds of events to the RODis not a problem as each DSP process the data coming from two inputs and each DSP works uncorrelated from others.

D. ROD and injection crates

Two crates were used during the ROD production. The first one was utilized as an injection crate, while the second one as a ROD crate. The crates used in the ROD productions tasks were WIENER VME -64x Series 6000 LHC and the Single Board Computer selected as the VME ATLAS ROD Crate Controller (RCC) was the VP 110/01X from Concurrent Technologies. With these crates and RCCs we had VME access to every board inserted in the crates.

The injection crate was composed by a TTCvi for trigger configuration, an OMB 6U as data generator and the OB as a

data repeater. In this case, the RCC was used for the configuration of the TTCvi and the OMB. In addition, a TTCex and a ROD Busy Module were used in order to test the RODs with the whole TileCal data acquisition system

The ROD crate contained the RODs to be tested, the TMs and the Trigger and Busy Module (TBM) to collect the busy signal from all the RODs in the crate and to make the veto to the trigger.

E. Computers and software

Three computers were used during the production for configuration tasks, acquisition and for data checking. The software utilized in the configuration of the tests was the ATLAS Trigger and Data Acquisition official software (TDAQ) adapted to our production tasks [4].

One of the computers was used to run the main partition of the TDAQ software. The TDAQ presents a graphical user interface and it was utilized for the configuration of the tests (Figure 5). A set of user defined applications for the TDAQ handled the CRC error checking during the dynamic tests. The results were displayed in another DAQ panel were the number of errors detected during a run was shown. Other information like number of run, integrated time, number of events processed, etc., was shown in the same display. Besides, when a run was finished another user defined panel stored all this information in the ROD production database (see section J).

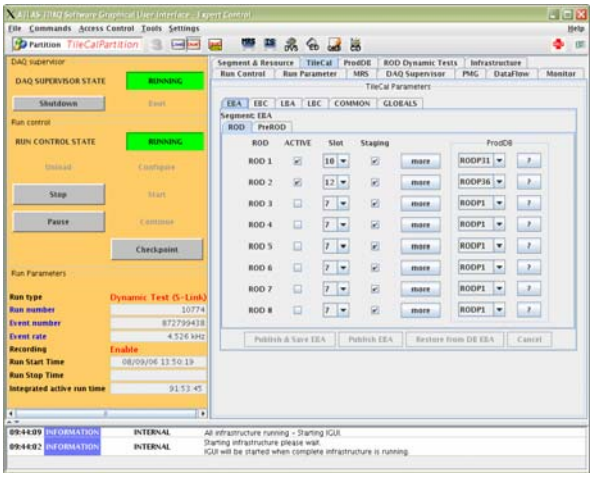

Figure 5: TDAQ software graphic user interface.

Two more computers were used for data acquisition and data checking coming from the ROD system. The first one was a dual CPU with 2 Four Input Links for Atlas Readout (FILAR) cards installed. These 2 FILAR cards read out up to 4 RODs, and store the data in a shared file system. The second computer, with access to this shared file system, checked the data online.

III. PRODUCTION TESTS

The ROD validation was divided into two different phases. In the first one, all the ATLAS calorimeters common RODs have been tested. These tests were made at the industry level and at the University of Geneva. Afterwards, the RODs were adapted to TileCal requirements and finally validated with this configuration.

F. Tests to ATLAS calorimeters common RODs

The ATLAS calorimeters common ROD motherboards were made in TechCI (France), and the components assembly in Seisystem (Italy). The RODs were delivered from industry with some general tests and mechanical checks. With the PUs already installed in the ROD motherboard, some JTAG boundary scan tests were made to the system. Nevertheless, the PUs were checked with X-ray tests previously to its insertion in the ROD motherboard. If all these tests were passed, the RODs were delivered to the UniGe, responsible of the validation of ATLAS calorimeters common RODs [2]. The UniGe group developed several functionality tests in order to check the correct dataflow across the boards. For this purpose, some static tests were made to prove the correct operation of programmable devices. Then, some data path tests proved the correct communication between the StagingFPGA and the OC. Finally, dynamic tests with the ROD Injector as data generator, and the TMs for sending the data out, validated the whole ROD system. These dynamic tests were made at different frequencies of injection and operating in full and staging mode.

G. TileCal adaptation

Once the ATLAS calorimeters common RODs were validated at the UniGe, they were delivered to the TileCal group. Then, the first task was to adapt them to TileCal specifications, including hardware and firmware modifications in the boards [1]. The hardware modifications were made at the electronic laboratory at IFIC-Valencia and they include some changes of clocks and passive components in order to adapt the G-Link frequency of data reception. The number of PUs utilized in TileCal RODs was also adapted as only 2 PUs per ROD are used in TileCal (Staging mode), instead of the 4 used in the Liquid Argon (LAr) subdetector (Full mode) [1].

Once the hardware modifications were done and with the boards already in the ROD crate, the firmware adaptation was realized. The specific firmware for TileCal was downloaded in the StagingFPGA, InputFPGA and in the DSP. Besides, the common firmware was updated as upgrades were available.

H. Validation tests of TileCal RODs

The ROD validation protocol consisted of a four level test chain. Each ROD had to pass all the test levels in order to be validated. The first level, called level 0, was basically a static test composed of three Diagnostic and Verification System (DVS) tests. These DVS tests basically certified the correct access through VME to every register inside all the programmable devices on the ROD motherboard. Besides, the correct communication between the StagingFPGA and the OC was checked sending several events from the internal memory of the StagingFPGA and reading them out with the OC. In order to consider the level 0 approved, each ROD had to pass at least three DVS tests.

Once a ROD has passed the level 0 tests, 3 levels of dynamic tests level 1, 2 and 3 are applied to the module. In these tests the OMB 6U board emulated the FE injecting data to the RODs. The data processed by RODs was stored and checked in the computers. The maximum trigger rate reached

by the online check task was approximately 400 Hz. For higher rates, the software couldn't check all the events in online mode, and only a percentage of the processed events were checked.

Level 1 test was a single ROD dynamic test at low rate. The trigger rate was 200 Hz and all the events passing across the ROD were checked. After more than 4 hours processing data without errors, the level 1 became approved. At that rate, no busy signals appear in the ROD system.

Level 2 test was also a single ROD dynamic test, but increasing the injection rate and number of hours of the run. In that case, the rate of the trigger was 1 KHz and only a 40% of processed events were checked. Besides, some busy signals appeared caused by the storage of data coming from RODs. Thus, the correct busy handling was also checked in that test. The ROD had to process data without errors at least during one hour in order to pass the level 1 test.

Finally, the level 3 test was a multiple ROD burning test at high rate. In this case, four RODs were tested together during at least 72 hours. The trigger rate was selected to be 1 KHz, and only 10% of the processed events were checked.

If no errors were found during the 4 level tests, the ROD became validated and ready to be installed in the ATLAS electronics cavern (USA15) at CERN.

Table 1: Four level tests protocol.

LEVEL	RODs	RATE	MINIMUM TIME
0	1	Three DVS tests	
1	1	200 Hz	4 h.
2	1	1 KHz	8 h.
3	4	1 KHz	72 h.

I. Data checking algorithms

The data processed by the RODs was checked online by two monitoring task algorithms. If the counter mode was selected in the OMB inside an event, all the words were equal and their value one unit higher than in the previous event. Through this check the ROD processing, it was verified the correct functioning of the ROD system.

In addition, as the OMB sent the CRC of each event attached as last word, it could be checked after the acquisition chain. The type of CRC utilized for data checking in ROD production was CRC-CCITT16. This type of CRC is also used in the TileCal experiment in order to check the correct data transmission between the FE and the RODs. The full configuration of the CRC utilized is showed in Table 2.

Table 2: Specifications of the CRC utilized in the RODs production.

Width	16 bit
Poly	1021 This is the divisor polynome
Init	FFFF This is the initial value of the register
Refin	CRC output is not reflected
Refout	CRC output checksum is reflected
Xorout	No XOR is performed to the CRC output
Check	ascii string "123456789" checksum is 29B1

J. Production database

After their adaptation to TileCal requirements the RODs, PUs and TMs were labelled and introduced in a database. Each ROD motherboard had associated two PUs and one TM. The validation of a ROD implied the validation of the entire group, which is labelled with a final ROD (RODF) label. This label can be seen in the front panel of each validated ROD (Figure 6). RODs are installed in the pit according to the component association introduced in the database.

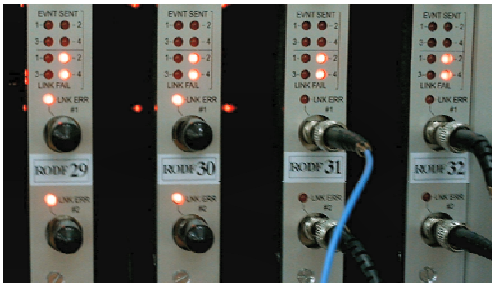

Figure 6: Final label in the ROD front panel.

The production database includes all the information about a ROD group. Besides, with the TDAQ software it was possible to save in the production database all the information related to each run. Thus, apart of the PUs and TM associated to each ROD and the firmware version of each programmable device inside a ROD, the production database includes all the tests done to every ROD.

Finally, the incidences found during the production were also introduced in the production database. Besides, the production database is totally accessible from a web page and as we have seen contains all the information about the ROD production.

IV. TESTS RESULTS

The number of ROD boards produced has been 38. For the read out of the experiment 32 boards are needed, and 6 units have been produced as spares. All the RODs produced have passed all the four level tests previously shown. It implies that each ROD has been processing data during at least 84 hours, has processed more than 264×10^6 events with at least 38×10^6 checked events without errors. Nevertheless, some extra runs were done during the production period in order to validate some firmware upgrades. All the runs were introduced in the production database and all they are counted as processing time by the RODs.

Table 3 summarizes the tests results in terms of time, events processed and events checked in the three different level tests during the RODs production.

Table 3: Summary of tests.

	Level 1	Level 2	Level 3	Extra runs
Time (h)	259	405	2001	560
Processed events	269×10^6	2040×10^6	8112×10^6	2708×10^6
Checked events	269×10^6	395×10^6	781×10^6	280×10^6

Nevertheless, during production tests some functioning problems were found in various RODs. Different kinds of problems were found, but all of them were detected and solved. In order to solve the problems found, one Optical Receiver in RODF24 and one DC/DC converter in RODF30 were replaced. Besides, the RODF25 had a scratch over a data bus and it was repaired. These repaired RODs were revalidated after their reparation.

Considering all the tests done during the production period, the ROD system has been processing data during 3225 hours. A total of $13129x10^6$ events were processed during this time, and $1,7x10^9$ events were checked without errors. The events injected by the OMB 6U and processed by the RODs during the production emulated an actual 9 samples event (176@32bits words). Thus, taking into account the number of bits processed by the ROD system, we obtain a bit error rate (BER) better than 10^{-13}.

Nevertheless, as shown before the number of events processed by the ROD system during the production was approximately $1,7x10^9$, which represents a run of 5 hours of the TileCal experiment at full expected rate (100 KHz).

K. Temperature tests

Apart from validating the correct functioning of each single ROD, we had to validate the cooling system selected for the TileCal ROD crates. As we have seen, RODs were designed in common for all ATLAS calorimeters, LAr and TileCal. In both cases, data are sent from the FE serialized and is deserialized in the ROD through the HDMP-1024 G-Link chip receiver. However due to the much higher channel density of the LAr detector the G-Link chips have to be clocked at 80 MHz in the LAr design, to increase the required bandwidth. This is beyond the nominal specifications of the chip. Nevertheless, the LAr group demonstrated the correct functioning of this device clocked at 80 MHz if the temperature was kept below 35 ºC. For that purpose, a water cooling system was included in the ROD. For the TileCal requirements, the G-Link is clocked at 40 MHz, well within the manufacturer specification, and it was decided not to use the water cooling system in TileCal and to use air cooling instead. In order to verify the correct functioning of the air cooling system some temperature studies were realized in the laboratory and in the pit. For these studies, the final composition of ROD modules per crate to be used at the pit was emulated, i.e., with 8 RODs and 8 OMB 9U boards in a ROD crate. As the OMB 9U are not so far available, we emulated this situation plugging 16 RODs in the same crate. Firstly we proved that the air cooling system worked better in the pit than in the lab. In addition, for the tests done in the pit the temperature of all the G-Links after more than 48 hours processing data was kept below 60 ºC, which is well within the chip specifications (85ºC). Apart of that, from these studies we concluded that the air cooling system doesn't work exactly in the same way in all the slots, and even for all the G-Links in a ROD (Figure 7). Regarding the slot, due to its position related to the fans, slot 18 was the worst cooled. Inside a ROD, the G-Links corresponding to the receiver 2 and 3 were the warmest.

With these results, the StagingFPGA firmware was modified in order to set the temperature threshold for the LED in the front panel of the ROD at 65ºC. At this temperature the ROD should work correctly but we considered that this temperature in any G-Link implies a wrong functioning in the cooling system.

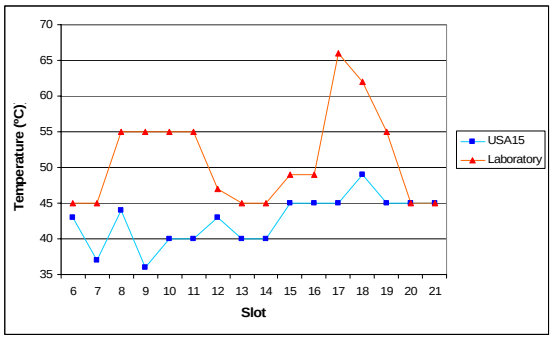

Figure 7: Temperature in G-Link 2 in all the slots of the crate, in the lab and in USA15.

V. Conclusions

The TileCal ROD production has consisted in the fabrication, adaptation to TileCal specifications and validation of 38 RODs. The validation procedure was applied to a complete ROD system composed of a ROD motherboard, two PUs and one TM, which will be installed together in the ATLAS cavern at CERN. A complete test-bench was designed for the ROD production and it continues being utilized on the DSP reconstruction routines tests since it is possible to emulate the front end with real data. Besides, some other firmware upgrades can be developed utilizing the data injection in the test-bench.

During the TileCal RODs adaptation and validation tests some performance errors were found, which were detected and repaired in all the cases. Besides, considering all the burning tests done during the production period, it was concluded that in the ROD system the BER is better than 10^{-13}. This BER is better than the specifications as the G-Link chip manufacturer certifies a BER of 10^{-12}. In addition, the burning tests verified that the air cooling system is enough in TileCal conditions.

All these results are being corroborated during the TileCal commissioning, where the RODs are being integrated in the ATLAS data taking system. Real data from TileCal front end are being processed by the ROD system and successfully analyzed offline.

VI. References

[1] J.Castelo et al., "TileCal ROD Hardware and Software requirements," ATLAS Internal Note ATL-TILECAL-2005-003, Feb. 2005

[2] LAPP Annecy and UniGe, "The ROD Test-bench description". Available: http://wwwlapp.in2p3.fr

[3] V.González et al., "Development of the Optical Multiplexer Board Prototype for Data Acquisition in the TileCal system" IEEE TNS, VOL.53, NO.4, August 2006.

[4] G. Crone et al. , "ROD crate DAQ User's Guide," ATLAS EDMS Document ATL-DQ-EN-0020, Sep.2005.