On the development of the final optical multiplexer board prototype for the TileCal experiment

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Abstract

This paper describes the architecture of the final optical multiplexer board for the TileCal experiment. The results of the first VME 6U prototype have led to the definition of the final block diagram and functionality of this prototype. Functional description of constituent blocks and the state of the work currently undergoing at the Department of Electronic Engineering, in collaboration with IFIC-Valencia, is presented. As no board is yet produced, no experimental results are presented but, nevertheless, design issues that have been taking into account as component placement and signal integrity issues will be detailed.

I. INTRODUCTION

TileCal [1] is the hadronic calorimeter of the ATLAS [2] detector at LHC [3]. Speaking in term of electronic systems, it consists of roughly 10000 channels which are read at the LHC bunch crossing rate (25 ns).

ATLAS trigger system is built around a multilevel concept which reduces the data acquired from the detector from 50 TB/s to 10-100 MB/s thanks to the low effective production cross section of the particles searched. Figure 1 shows the block diagram of the trigger system. Level 1 is detector dependent because it has to adjust to their particularities while level 2 and 3 are common to all subdetectors in ATLAS.

In the interface between levels one and two, data gathering according to physical phenomena takes places and, depending on the detector, also data preprocessing can be performed. This functionality, among others is part of ROD (Read Out Driver) systems [4].

For the Tilecal ROD system, channels are gathered, at this level, following the trigger towers and data is preprocessed calculating, in real time, the energy, timing and χ2 values using digital signal processing algorithms. These values for all the channels are sent to second level processors for further decision. The ROD system will be built with 32 custom VME boards which will treat around 2 Gbytes/s of data (300 channels per board). The basic schema used is based on the ROD crate concept in which ROD modules are grouped into VME crates jointly with a Trigger and Busy Module (TBM) [5] and possibly other custom cards when needed. This ROD crate interfaces with the TileCal Run Control and the ATLAS DAQ Run control.

TileCal FrontEnd electronics is placed inside the detector. This makes the system sensitive to radiation produced by the particle collisions. In this sense, ATLAS specifications require the electronics to work properly for a period of 10 years.
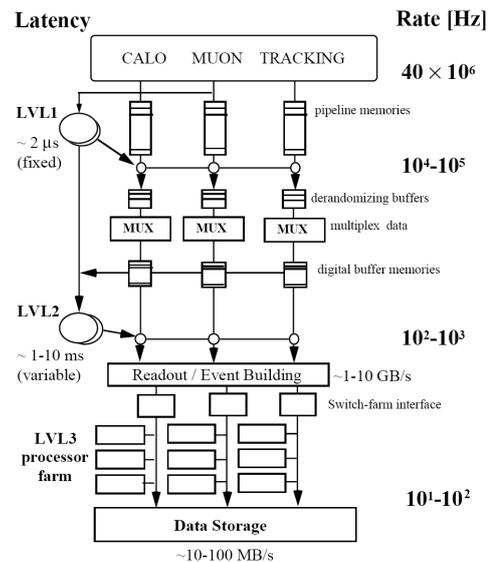

Figure 1: The ATLAS three levels trigger system.

TileCal electronics will receive about 2 Gy/year (0.2 Krad/year) of radiation for a total dose of 20 Gy in the experiment lifetime [6]. To measure radiation hardness of TileCal FrontEnd electronics, tests were conducted with proton beams in different areas and with different beam sizes. Thanks to these tests, three non-destructive kinds of errors were found:

• Transient error in the data flow out to the ROD.

• Permanent errors in the data flow requiring reset.

• Latch-up error with an increment in current consumption of 60 mA.

To reduce data loss due to radiation effects, the TileCal collaboration decided to include data redundancy in the output links of the FrontEnd. This was accomplished using two optical fibres which transmit the same data. At ROD system level, data redundancy is used to discard the fibre with errors due to radiation. The checking is based on rightness of the Cyclic Redundancy Codes (CRC) of the data packets on both fibres. This is also necessary as the ROD motherboard is expecting just one fibre per channel. For this purpose a new module, called PreROD or Optical Multiplexer Board (OMB) was conceived.

In this way, the Tilecal ROD System is subdivided into two subsystems:

- The ROD motherboard [7]
- The Optical Multiplexer Board [8]

The ROD motherboard contains the full processing capability for the estimation of energy and time on data coming from the FrontEnd while the OMB will perform data checking looking for transmission errors due to radiation.

II. OPTICAL MULTIPLEXER BOARD 6U PROTOTYPE

The OMB 6U Prototype was conceived as a first experience with the implementation of the functionality of this system. Besides, in the course of the work, a Data Injection Mode was added as a way of testing the ROD module in production phases or whenever there is no FrontEnd available. It has been designed as a VME64x slave module architecture including four optical inputs connectors (two input channels) and two optical outputs connectors integrated in the PCB. The input channels are capable to read up to 4x16 bits at 40 MHz. The output also runs at 40 MHz with a data width of 16 bits.

The error check is based on the real time calculation of the CRC value of the data received on both input fibres. Once calculated, this value is compared to the one included within the data. If the values differ, then the fibre is carrying defective data. Decision logic then selects which fibre will provide the data to the ROD motherboard taking into account the results of the CRC checking. In Data Injection Mode, data can be preconfigured or dynamically loaded using VME bus and injected with an internal or external trigger signal.

There are four input G-Link chips (Agilent HDMP-1034) [9] on the board, two output G-Link chips (Agilent HDMP-1032) [9], two FPGAs for CRC calculations (CRC FPGAs) and one FPGA for VME interface (VME FPGA). These lasts are implemented in ALTERA devices. Furthermore, for the Data Injector Mode, the OMB has two additional copper input cables for trigger and busy signals coming from the ROD motherboard. These external signals are included in this prototype to send correctly internal data in order to test the ROD functionality.

The block diagram of the board is shown in Figure 2. A short description of the main functions of the G-link and FPGA chips in the OMB board is given in Table 1.

Table 1: OMB main components

Components	Main Function	Chip
6 G-Link Chips	Serialize/deserialize the outcoming/incoming data.	HDMP-1034 HDMP-1032
2 CRC FPGAs	Send correct data to ROD. ROD Injector Data.	CYCLONE EP1C12
1 VME FPGA	VME Interface. OMB control.	ACEX EP1K100

1) Input/output hardware

Infineon optical transceivers [10] are used for input and output optical links. There are four optical fibres coming in from the FrontEnd Boards (FEB) and two optical fibres going out to the ROD. G-link chips (HDMP-1034 and HDMP-1032) are used in the input and output stages. The HDMP-1034 deserializes the input bit stream and output it as a 40 MHz 16 bit word data flow to the CRC FPGAs (one per input channel, i.e. two input fibres). The output data of each CRC FPGAs is a 16 bit word stream at 40 MHz sent to the HDMP-1032 chips where it is serialized and sent to the ROD motherboard.
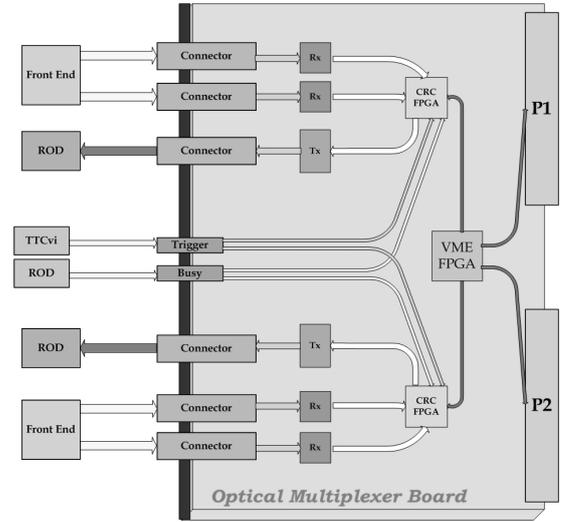

Figure 2: Optical Multiplexer Board Block Diagram.

2) FPGA Description

Two CYCLONE EP1C12 FPGAs [11] are used in the OMB board for CRC checking and link control. The incoming data from each pair of different G-link receiver chips is routed to one of these FPGA. Data is then analyzed, in parallel both input links, and the decision is made on which data link is the correct one. Each CRC FPGA routes the correct data to its G-link transmitter chip.

If the OMB is working in Injection Mode then only the output fibres (and the corresponding serializers) are used. In this mode the data to send is preconfigured in the CRC FPGA firmware or stored in an event memory using VME bus transactions. The user can choose how to trigger these data: either externally (using NIM level signals) or internally thanks to a trigger generator programmed inside the VME FGPA. Once triggered, data is sent either to one or both of the CRC FGPA which sends them to ROD motherboard. The data injection can be stopped externally, if programmed in this way, by means of a Busy signal.

VME interface is controlled by an ACEX EP1K100 [12] FPGA chip present in the OMB. The OMB module is considered as a VME slave module and all actions and commands are controlled by the crate CPU following the VME64 standard.

VME map includes registers holding the number of CRC errors detected in the optical fibres, control registers to select CRC checking or injection mode and an event memory to load the data for injection. The addressing mode is A32D32. A 16-bit bidirectional bus connects the VME FPGA with the two CRC FPGAs.

All the FPGA firmware in the OMB was developed with Altera Quartus II software [13].

3) OMB implementation

The OMB was built using a 12 layer PCB. The layer stackup was designed to minimize crosstalk between layers by routing the adjacent ones orthogonally. Each two internal layers are between power or ground planes for this same reason. Optical transceivers and serializers/deserializers chip signal are preferably routed on the top layer for faster signal transmission. Buses are routed in parallel with equal trace length for minimization of skew. Figure 3 shows a photograph of the OMB finally implemented.
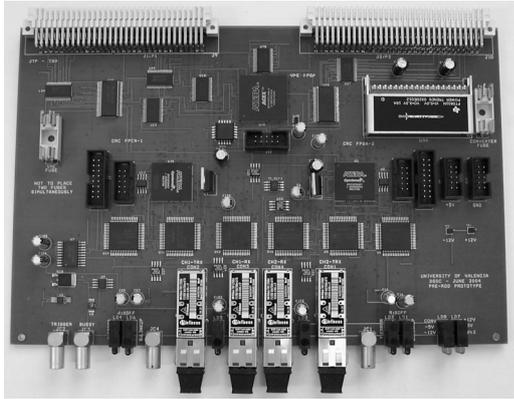

Figure 3: The Optical Multiplexer Board prototype.

III. OMB 9U FINAL PROTOTYPE

The good results achieved with the 6U experience are being now used to define the final OMB prototype. This prototype is conceived in a 1 to 1 ratio with respect to RODs. This means that each final prototype will have 8 input channels (16 fibres) and 8 output channels (8 fibres). Due to this modification a 9U format has been chosen for this new implementation.

With respect to functionality there are some minor modifications among of which, the inclusion of the TTC receiver chip is the main one. This would lead to the possibility of having trigger directly from the TTC system, something which is not possible now.

In view of future upgrades and functionality the design includes four PMC connectors for mezzanine boards connected to CRC FPGAs and is being designed for 80 MHz operating frequency instead of the nominal 40 MHz of LHC.

This last issue poses some problems related to signal integrity and component placement aspects. Among them, the use of a single JTAG chain for the programming of all the FPGA chips in the board, the bus connecting the VME controller and the CRC controllers and the clock distribution are the main concerns. Simulations of these connections as well as firmware modification in the FPGA used are part of the work currently going on.

A. Board Description

Figure 4 shows the block diagram of the final 9U prototype including the modifications mentioned above.

Stratos Ltd. dual optical receiver (M2R-25-4-1-TL) and transmitter (M2T-25-4-1-L) [14] have been chosen to optimize the space in the board.
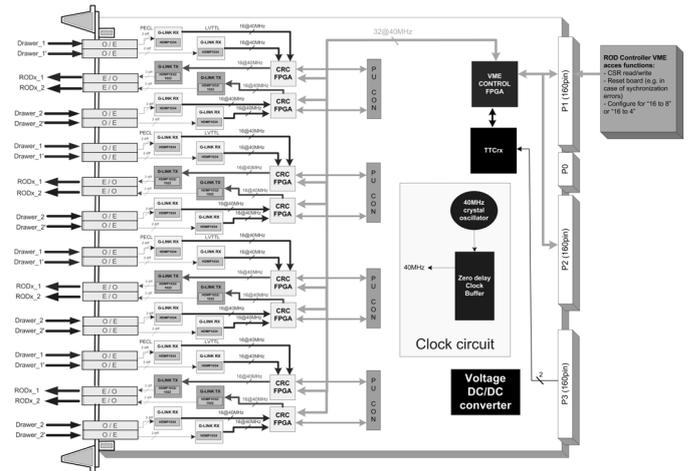

Figure 4: OMB 9U prototype block diagram.

For the CRC FPGAs we use the CYCLONE EP1C12 used in the previous 6U prototype. However, the VME FPGA has been changed from the ACEX FPGA to a CYCLONE EP1C20 FPGA. The reason for this change is that the final prototype includes a TTCrx [15] receiver chip. For this chip, special control firmware must be present in the board. In order to keep the number of components to a minimum we have decided to put this firmware inside the VME FPGA. In order to not compromise the occupancy of the FPGA we have chosen an FPGA with even more logical components than the CRC FPGA.

Figure 4 also shows the four PMC connectors placed in the board which connect to each two CRC FPGAs. The idea behind this decision is twofold: we have plenty board space and, if needed, daughter boards might be plugged in to do some processing tasks on data sent by the CRC FPGAs.

For what respects to functionality, the final prototype keeps the presently available in the 6U prototype except for the possibility of receiving TTC signals. This means that the OMB will be able to inject data on the basis of an external trigger signal or VME command, including real trigger information.

B. PCB description

The OMB final prototype layout is a 10 layers PCB which optimize cross-section to minimize signal integrity problems. Figure 5 shows the arrangement of layers. We tried to keep every signal layer between two power planes or, when it was not possible, routing the two adjacent layers orthogonally. Layers TOP, INT1, INT2, INT3, INT4, BOTTOM are signal layers while PWR1, GND1, GND2, PWR2 are power layers.

Power distribution is also a concern in this board as we need several different supply voltages. For all the FPGAs we need 3.3 V for the I/O while internal operation needs 1.5V. The NIM to TTL conversion for the external trigger signals need a 12V supply voltage while other logic circuitry needs 5 V. The 12V and 5V power supplies are taken from VME bus or, when not available or for testing, from special pins on the board. Generation of the lower voltages (3.3 V and 1.5 V) is

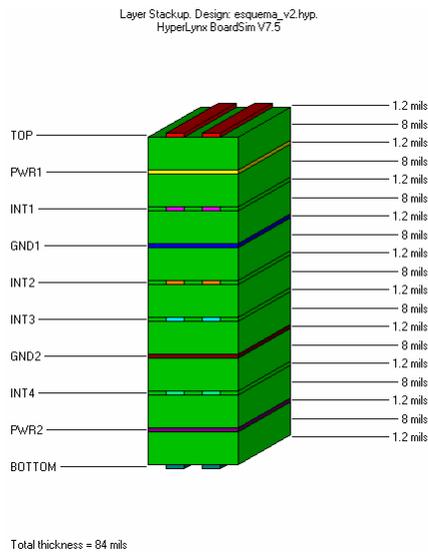accomplish by voltage regulation from the 5 V main power supply.

Figure 5: OMB 9U Prototype layer stackup.

With this configuration, we chose to assign PWR1 plane to 3.3 V while PWR2 is a split plane with a main 5V area and a 1.5V island (figure 6).
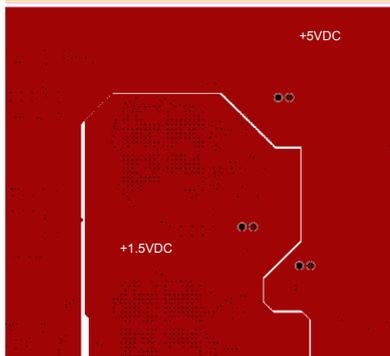

Figure 6: PWR2 split power layer detail.

C. Signal integrity analysis

As it was previously mentioned, signal integrity analysis is one of our main concern in the design of this prototype. In this sense, the three main signal distributions to be aware of are the JTAG chain, the clock distribution and the serial bus. Differential lines connecting the optoelectronic connectors and the GLINK chips are also of great importance. However, close placement of chip to connectors and parallel manual routing of the lines assure signal quality.

Because our work is still under development only the analysis of the serial bus will be presented here. This bus has a CLK signal and 3 data lines. In principle, we would only use one of the data lines. The other 2 data lines will be used if an increase of bandwidth is needed.

The key point is this analysis is how to route and terminated properly this bus. We test three different routing and termination schemes and analyzed them with Cadence PCB Studio and SigExpert tools [16].

The first attempt was to route the bus from the VME FPGA to a point between the first and second CRC FPGA. All these FPGA will be place in a column along the board width. Figure 7 shows this configuration.
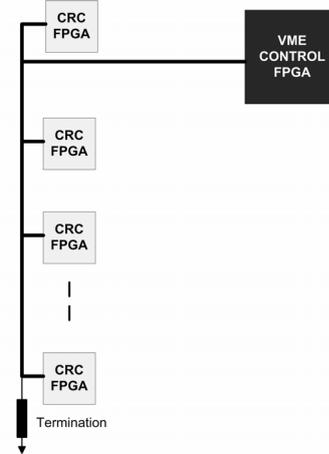

Figure 7: First routing scheme from VME to CRC FPGAs.

After topology extraction, simulation of the bus signals was carried out. The results are displayed in figure 8.
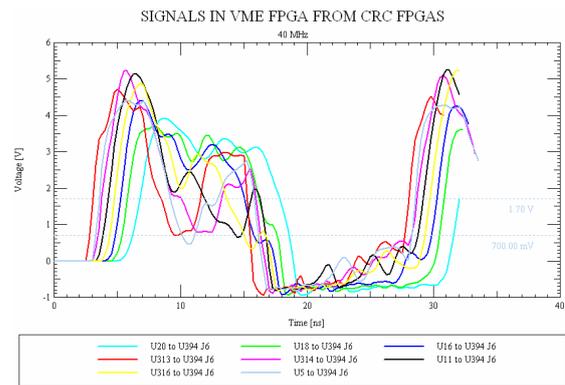

Figure 8: Simulation results of the first configuration

It is clear that the results are everything but satisfactory as several signal cross the logic thresholds even more than once. The reason for this behaviour is the "T" junction that appears when the lines coming from the VME FPGA get to the ones connecting all the CRC FGPA. This junction creates reflections which travel all along the line. Also reflections at the top FPGA travel down the bus creating interferences.

A better, but not too much, behaviour is accomplish is the routing is designed so signals travel along all the CRC FPGA from top to bottom, as figure 9 shows.

Simulation results of this configuration are shown if figure 10. We may observe a little improvement in signal quality but these results are far from optimum.

From this point we analyzed the termination scheme. In the literature bidirectional buses like this one are generally terminated using serial resistors at the output of all the devices attached. However this generates an staircase waveform in the middle of the bus. In our case, data go from an to the VME FPGA but not among the CRC FPGA so, strictly speaking this bus is not full bidirectional.

Analysis of this special case with SigExpert showed that the best results are achieved when one termination resistor is

placed at each end of the bus, i.e. one at the VME FPGA output and one at the bottom CRC FPGA (figure 11). The value of this resistor is 50 Ω.
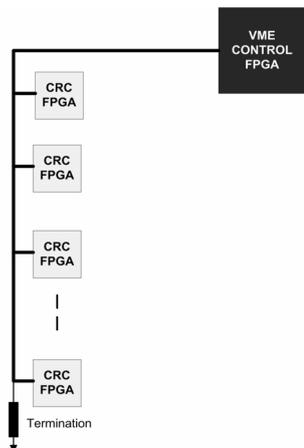

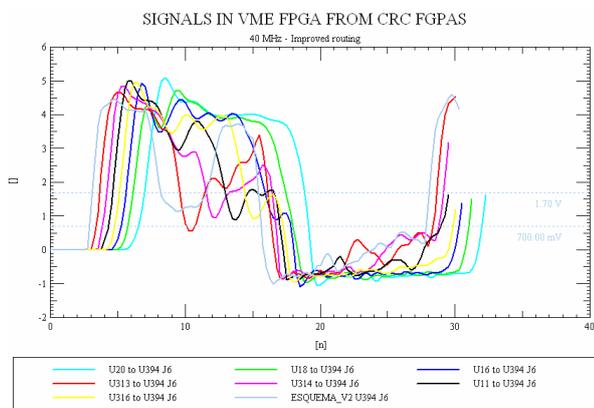Figure 9: Second routing scheme from VME to CRC FPGAs.

Figure 10:   Simulation results from the second configuration.

With this termination setup results are greatly improved as it is shown in figure 12. This means that the correct routing will be from top to bottom CRC FPGA with two resistors placed at both ends of the bus.

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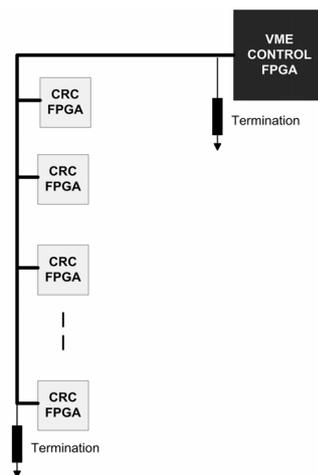
Figure 11:   Final routing scheme of the serial bus.
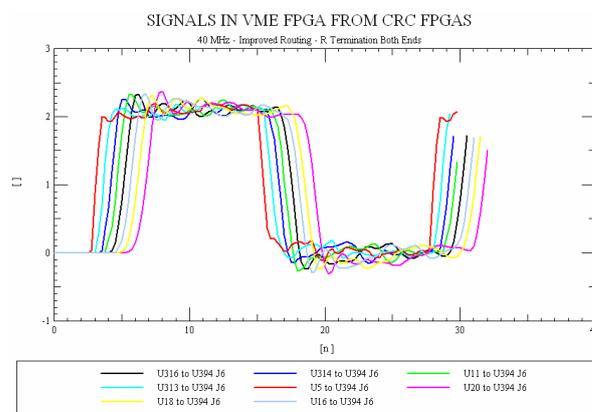

Figure 12:   Simulation results of the final configuration.

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V. ACKNOWLEDGMENTS