Real Time Data Processing of the TileCal Calorimeter of the Atlas Detector

A. Munar*, J. Castelo*, C. Cuenca*, A. Ferrer*, E. Higón*, C. Iglesias*, J. Poveda*, A. Ruiz-Martínez*, B. Salvachuà*, C. Solans*
*Departamento de Física Atòmica, Molecular i Nuclear and IFIC, CSIC-Universitat de València
Apdo 22085 E-46071 València - Spain
Email: antoni.munar@ific.uv.es

V. González†, J. Torres†, J. Soret†, E. Sanchis†, J. Martos†, J. A. Gómez†
†Electronic Engineering Dept., University of Valencia-ETSE, Burjassot (Valencia), Spain.

***Abstract*— The TileCal detector is an iron-scintillating fiber sampling calorimeter of the ATLAS experiment, one of the experiments at the Large Hadron Colloider (LHC) accelerator at CERN (European Laboratory for Particle Physics), scheduled to start in 2007. At a Level 1 Trigger rate of 100 kHz, the Read Out System of the TileCal has to be able to process and format the data of 10.000 read-out channels (112.91 Gbps of input bandwidth) in 2 μs to avoid dead time. Furthermore, to reduce the amount of data and to meet the maximum output bandwidth of the Level 2 Trigger of 53.7 Gbps, real time computation of the deposited energy applying optimal filtering techniques and collision time computation must be performed for each channel. This is accomplished with a Read Out Driver system of which 32 9U VME boards are the main components. Each board consists of 8 G-links receivers and 4 S-Link transmitters, and 8 Digital Signal Processors (Texas Instruments TMS320C6414@600 MHz DSP), totalizing 68992 MIPS of processing power. These boards are presently at the production stage.**

We report on the overall design of such system, using the DSP for energy and collision time computation, data formatting, and identification of low transverse momentum muons in real time with high efficiency.

I. Introduction

At CERN (European Laboratory for Nuclear Research, Geneve, Switzerland), in 2007 the *Large Hadron Colloider* (LHC) will deliver proton-proton collisions at center of mass energies of $\sqrt{s} = 14$ TeV with luminosities in excess of 10^{34}c $^{-2}$ $^{-1}$. Two general purpose particle detectors, ATLAS (*A Toroidal LHC Apparatus*) and CMS *Compact Muon Solenoid* will provide the necessary instrumentation for the study of such proton-proton collisions, to probe the most fundamental laws of matter and, hopefully, making discoveries leading to new physics.

The LHC bunch crossing frequency is 40 MHz, and therefore collision data must be collected every 25 ns. With a such short bunch spacing and with the required high luminosities, on average 25 (Poisson distributed) proton-proton collisions will occur at each bunch crossing. To achieve the necessary performance, the readout system must fulfill the following three requirements: 1) Detector responses are in same cases of the order of microseconds, and therefore fast ($\approx$ ns) shaping and digitization is needed 2) With input data rates of 40 MHz and to tape data rates of $\approx$ 100 Hz, a data rejection factor of 10^7 is necessary to keep only potential interesting events, and must be performed with on-line algorithms. Another non-trivial issue is the implementation of an efficient architecture for the readout of millions of readout channels 3) Due to the high luminosities and extremely short bunch spacing, effects that greatly deteriorate the detector performance like energy pile-up must be filtered in order to allow an optimal trigger performance. The ATLAS readout system has been designed to meet these three requirements.

We report on the general structure of the readout system of the hadronic calorimeter of ATLAS TileCal[1], the design and architecture of the central part of the TileCal Readout System the Read Out Driver board (ROD), the functionality of the ROD embedded processing units (PU), where the data is formated, synchronized, and the energy for each channel is computed with optimal filtering techniques. Due to the processing power of the PU, we report on other on-line requirements, like the on-line computation of the missing transverse energy and the implementation of an on-line low p_T muon trigger at Level 2. Finally, first experience on production tests and preliminary integration is reported.

II. The TileCal Readout System

The Hadronic Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS detector. It is an iron-scintillating plastic calorimeter (Figure 1) of approximately 12 m long, with the shape of a hollow cylinder with an inner radius of 3 m and an outer one of 5 m, approximately. The light produced in the scintillating tiles is driven to the Hamamatsu photomultipliers by Wave Light Shifting (WLS) fibers. The detector is segmented in azimuth in 64 equal size wedges, while in pseudo-rapidity η [1] it is divided in four barrels spanning $-1.2 < \eta < 1.2$. In total, the TileCal has 9856 readout channels. Each channel corresponds to a single photomultiplier. The photomultiplier signal is sampled each 25 ns and digitized with 10-bit precision. To cope with the huge

[1]The reference system is such that the detector has cylindrical symmetry around the beam axis where θ is the polar angle. The pseudo-rapidity, a convenient magnitude in particle physics, is defined as $\eta = -\ln(\tan(\theta/2))$.

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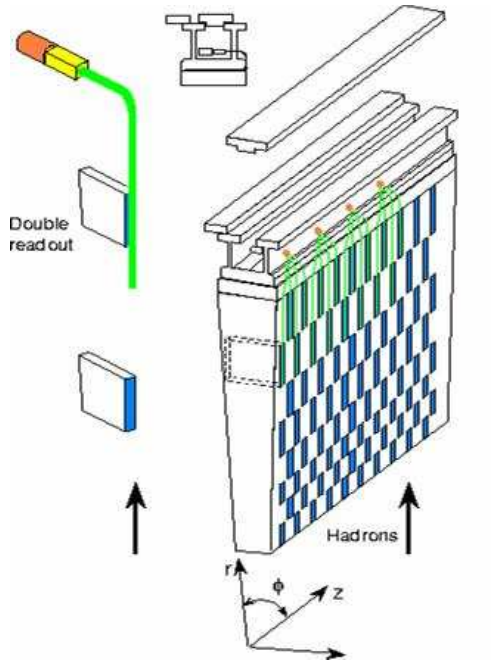

Fig. 1. Schematic view of one wedge (1/64 in azimuth) of the TileCal calorimeter. Shown are the plastic scintillator tiles, embedded in the iron passive material, and the WLS fibers carrying the light generated by the ionizing particles in the tiles to the readout photomultipliers.

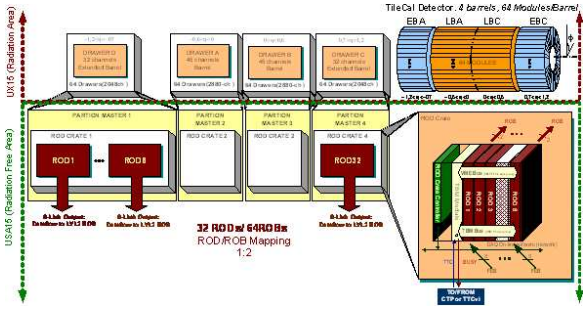

Fig. 2. Logical view of the TileCal readout scheme. The detector is divided in four partitions, each corresponding to a barrel (EBA, LBA, LBC, EBC) of the detector. Each partition is housed in a ROD crate with 8 ROD boards, with its own Partition Master (a single board computer) and its own synchronization unit, a separated TTC crate.

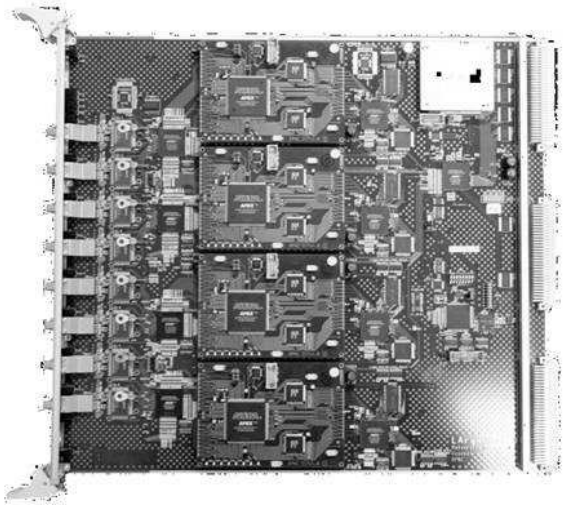

Fig. 3. A view of the TileCal ROD motherboard from the top. Four processing units are shown plugged as mezzanine cards.

required dynamic range[2] (from 0 to 10 GeV -0 to 10 pC- and 10 to 1000 GeV -0 to 800 pC-) two gains (ratio 1/64) are implemented in the front end electronics by means of simple switches[1]. In ATLAS, the trigger system is organized as a three level system[2]. At Level 1, synchronous with the LHC clock of 40 MHz, the data is acquired, stored in a pipeline and crudely processed by the trigger system. At this stage, interesting events are selected at a maximum rate of 100 kHz. Upon the receiving of a Level 1 trigger accept signal, the TileCal front electronics sends out the data, consisting 7 samples[3], to the next stage of the Read Out System, the Read Out Driver (ROD). Taking into account that there are approximately 10.000 readout channels, the ROD system has to process up to 150 Gbyte/s.

III. The Read Out Driver

At the L1 rate of 100 kHz the data is transmitted from the front-end electronics, housed in the drawer of each wedge, to the Read Out Driver Board (ROD) by means of optical fibers. The front-end electronics is placed in a non radiation free environment. To avoid error transmissions due to single event upset and other radiation effects, the data path is duplicated and sent through two different optical fibers. In the counting room, a radiation free environment where the ROD is located, an specially designed board compares the data, checks for errors and sends it to the ROD through a single optical fiber[4].

[2]To be sensitive to minimum ionizing particles in the low end, and hadronic jets in the high end.

[3]This number is configurable depending on the physics requirements.

The TileCal readout is divided in four partitions, each one with his own Trigger and Time Control units for synchronization and trigger, so they can be operated as independent detectors (Figure 2). Each partition corresponds to a barrel of the detector, and for each barrel each single wedge is readout by one optical fiber.

The ROD motherboard is the core of the TileCal readout system. It is a standard 9U VME64x board (Figure 3). It was developed by the Liquid Argon Calorimeter Detector of the ATLAS collaboration[5], and modified to suit the TileCal readout requirements[3]. The input data is received by eight Optical Receivers. Each fiber carries the data of a whole module. There are in total 64 (azimuth) x 4 (in η) = 256 modules, and therefore 32 ROD boards are needed, distributed in four crates with 8 ROD modules each. After the optical receivers (Figure 4) the data is deserialized and distributed into four staging FPGAs, which re-routes the data to the processing units. This allows to use a variable number of processing units (2 or 4), depending on the computing needs or number of channels to process. After the data is processed in the processing units, a FPGA output controller

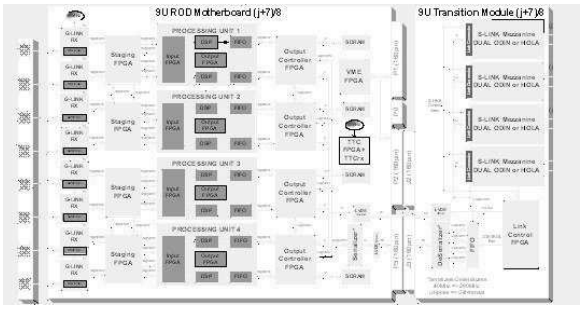

Fig. 4. Schematic view of the different functional components of the TileCal ROD motherboard[3]

may store the data in a SDRAM accessible through the VME backplane, or send it to the Transition Module (Figure 4), the later provided with S-Links to send the data to the general ATLAS data acquisition system. Signals inside the ROD board are LVTTL, while for the communication with the Transition Module LVTTL to LVDS serializers were used, as there were not enough pins in the P2/P3 backplane to handle the whole S-Link signals. Again, with the output controller one can re-route the data, and therefore the number of S-Links is configurable (2 or 4). The ROD also receives the trigger clock and related information through the P3 backplane from a dedicated module that receives such information by optical links. These signals are decoded and processed by a TTCrx chip and a TTC FPGA, where they are routed to the processing units for data synchronization. The ROD also handles through an FPGA the management of the BUSY signals, in case the data flow is stopped and the data buffers are full. The ROD board is an slave VME board. The VME bus can be used for the configuration of the motherboard devices, boot of the Processing Units, code download for the DSPs, and on-line access data, like histograms stored in the DSPs memory through the DSP Host Port Interface.

IV. The Processing Units

The DSP Processing Unit[6] is a mezzanine (120×85 mm) board equipped with two Input FPGA (Cyclone EP1C6), two TMS320C6414 720 MHz DSP (5760 MIPS) from Texas Instruments, two Output FIFOs, and an output FPGA. Data from the detector enters the input FPGA, where they are formatted and checked as needed by the DSP algorithms. When event data is ready, an interrupt is sent to the DSP which launches a DMA to read the data with the 64 bit EMIFA bus. After the DSP has finished processing an event, it writes the results in the output FIFO through the 16-bit EMIFB bus. The trigger information for data synchronization is received through the output FPGA, and sent to each DSP via the serial ports. DSP code download, memory check and on-line histograms (see Section V) are performed through VME via the Host Port Interface. Commands for the DSP Finite State Machine are sent through the multi channel buffered serial port. The processing unit also allows the dynamic on line configuration and boot of the input FPGA without system shutdown.

V. On-line Computing Requirements of the Processing Units

The ROD motherboard has been designed in such a way that it can be configured in two different modes depending on the required processing power or allowed cost. In normal mode, the ROD board is equipped with four processing units, and therefore each DSP carries out the data processing for the data coming through one optical input (Figure 4). In staging mode, the staging FPGA re-routes the data from four optical links, and sends it to one single PU. Therefore, one DSP processes the data from 2 optical links. The output can be configured also in analogous way, where the output FPGA controller sends the data of each processing unit to a single S-Link, or re-routes the data from two processing units to a S-Link, depending on the data bandwidth requirements. For the TileCal, at 100 kHz level 1 Trigger rate, it was found that the operation in staging mode is satisfactory, both from the point of view of needed data bandwidth and computing resources. Each optical fiber carries the data of 32 or 45 photomultipliers, which at 100 kHz trigger rate means an input bandwidth of approximately 500 Mbps per processing unit (two DSP), for a maximum of 640 Mbps. The estimated output bandwidth per processing unit is approximately 780 Mbps, for a maximum of 1,28 Gbs (limited by the output FPGA controller).

In staging mode, for each two optical links (90 channels in total), each DSP has to check the synchronization of the data with the trigger information, perform energy and time reconstruction applying optimal filtering techniques[7][4], output data formatting and on-line histogramming of the reconstructed energy, time and quality factor of the reconstruction[5] Such algorithms are currently been implemented in C and assembler. To avoid dead-time, the maximum allowed latency is $10\mu s$

Due to the processing power of the DSP two other task has been required to be implemented in the DSP. The first one is the computation of the Missing Transverse Energy. Due to the data unpacking latency at Trigger Level 3, it has been required to compute the Missing Transverse Energy for each module, and pack it as two words in the output data. In the DSP this can be implement by simply multiplying the energy of each channel by the c and 1 of each tower, by means of a look-up-table, downloaded in memory through the host port interface. A second task is the implementation of a low p_T muon trigger. Low p_T muons ($p_T < 2$ GeV/c) are detected by the ATLAS muon trigger with very low efficiency. On the other hand, muons, as minimum ionizing particles (m.i.p), have a very distinctive energy deposition signature in the TileCal. Due to the radial segmentation of the TileCal (Figure 5), a muon will deposit almost the same amount of energy in the three

[4]Since the planned time span of the experiment is 10 years, it was found that performing such filtering with the DSP it was the best way to provide the needed flexibility for a evolving noise environment (changing conditions, accumulated radiation damage, etc..)

[5]Such histograms can be readout asynchronously and in parallel through VME via the DSP host port interface.

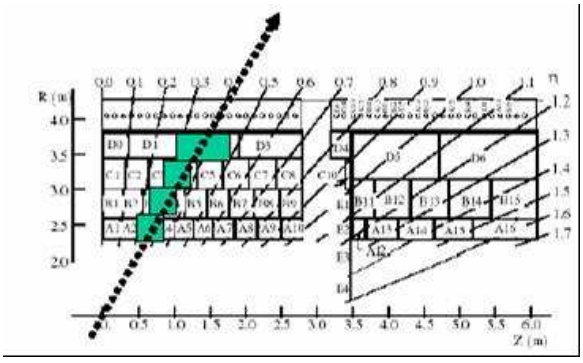

Fig. 5. Energy deposition pattern for a muon transversing the TileCal at a given pseudo-rapidity.

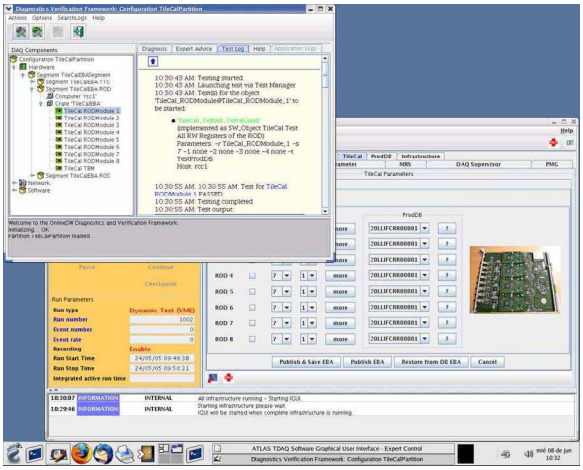

Fig. 6. Screen shot of the TDAQ software panel, showing several ROD mother boards under test.

radial segments, and therefore a simple pattern recognition can be implemented in the TileCal DSPs. Studies are underway to asses the feasibility of such algorithm in the TileCal ROD DSPs.

VI. Production System Tests

Extensive Tests had been performed at the level of single board checking data injection, data read through the VME bus ,and data read through the optical links[8]. It had been also successfully tested at the ATLAS test beam at the SPS CERN accelerator. At the present time, production tests have been started, with both the firmware and the DSP code under continuous upgrades and optimization. Pre-production boards had been successfully integrated in the ATLAS TDAQ system (Figure 6). The ATLAS TDAQ software[9] has allowed the operation of multiple RODs in distributed crate, with the management of different crate controllers, with a centralized logging system and data taking.

VII. Conclusion

In this paper, we present an overview of the data acquisition system of the Tile Hadronic Calorimeter of the ATLAS detector, the core component of which is the Read Out Driver mother board (ROD), together with its processing units. The DSP embedded in the ROD provide a flexible way to implement easily changing algorithms like pulse energy computation with optimal filtering, on line monitoring, on-line missing transverse energy computation and possibly low p_T muon triggering through pattern recognition of characteristic energy deposition in the TileCal calorimeter.

At the present time, production tests have been started, and firmware is under an intense development. A first integration of pre-production ROD modules in the general ATLAS DAQ system has been performed. Final installation in the ATLAS cavern is foreseen to take place in Autumn 2005.

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