Data acquisition in TileCal/ATLAS experiment. Design of the Optical Multiplexer Board Prototype

V. González, J. Torres, J. Soret, E. Sanchis, J. Martos,
Dept. Ingeniería Electrónica, Universidad de Valencia – ETSE

J. Castelo, V. Castillo, C. Cuenca, A. Ferrer, E. Fullana, E. Higón, J. Poveda,
A. Ruiz-Martínez, B. Salvachúa, C. Solans, J. A. Valls, A. Munar, C. Iglesias, A. Valero
I.F.I.C. – Centro Mixto Universidad de Valencia – C.S.I.C.

Abstract—**The Optical Multiplexer Board is one of the elements present in the Read Out chain of the Tile Calorimeter in ATLAS experiment. Due to radiation effects, two optical fibers with the same data come out from the Front End Boards to this board, which has to decide in real time which one carries good data and pass them to the Read Out Driver motherboard for processing.**

This paper describes the design and tests of the first prototype, implemented as a 6U VME64x slave module, including both hardware and firmware aspects. In this last, algorithms for Cyclic Redundancy Code checking are used to make the decision. Besides, the board may be used as a data injector for testing purposes of the Read Out Driver motherboard.

I. Introduction

CERN, the European Laboratory for Particle Physics, in Geneva, Switzerland, is working in new particle physics research. The next step in this research is the construction of a new particle accelerator, the *Large Hadron Collider (LHC)*. In the year 2007 beams of protons are expected to collide at a center of mass energy of 14 TeV. In parallel with the construction of the accelerator, two general purpose detectors, *ATLAS (A Toroidal LHC Apparatus)* and *CMS (Compact Muon Solenoid)*, are being developed to investigate proton-proton collisions in the new energy domain LHC will provide and to study fundamental questions of particle physics.

Each one of these detectors is composed of several subdetectors. TileCal, a hadronic calorimeter, part of ATLAS detector, is one of these. It will be prepared to read, in each collision, through thousands of electronic channels, a high volume of data. The integrated analysis of all the information provided by subdetectors poses new challenges in the development of new real time systems. The work presented here is included in the studies and development currently carried out at the University of Valencia and IFIC for the Read Out Driver System of the hadronic calorimeter TileCal of ATLAS.

II. TileCal ROD System

TileCal consists, electronically speaking, of roughly 10000 channels to be read each 25 ns. Data gathered from these channels are digitized and transmitted to the data acquisition system following the assertions of a three level trigger system [1].

In the acquisition chain, place is left for a system which has to perform preprocessing and gathering on data coming out after a good first level trigger before sending them to the second level. This System is the Read Out Driver. Fig. 1 shows this structure schematically.

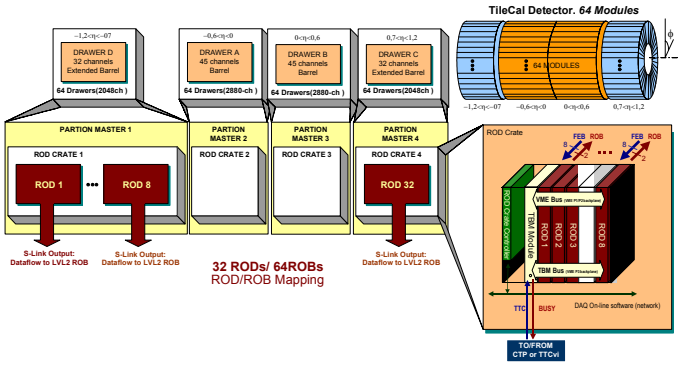

Fig. 1. TileCal ROD System.

For TileCal, the ROD system will be built around custom VME boards which will have to treat around 2 Gbytes/s of data. Intelligence will be provided to do some preprocessing on data. For the reading of the channels we are working on a baseline of 32 ROD modules. Each one will process more than 300 channels.

The basic schema to use is based on the ROD crate concept in which ROD modules are grouped into VME crates jointly with a Trigger and Busy Module (TBM) and possibly other custom cards when needed. This ROD crate interfaces with the TileCal Run Control and the ATLAS DAQ Run control.

For TileCal the ROD System are further subdivided in two subsystems:

- The ROD motherboard
- The Optical Multiplexer Board

The following sections describe the Optical Multiplexer Board.

III. Optical Multiplexer Board

TileCal is a redundant data acquisition system. Two optical fibres carry the same data from the front-end electronics to the ROD. This is necessary as radiation phenomena could cause malfunctions inside the front-end electronics and bit and burst errors over data ready to be transmitted to the ROD card. Nevertheless, the ROD motherboard card has only one input connector for each data link, as the original design responds to these initial specifications.

Our primary target is to improve the error tolerance, designing a pre-ROD card, called Optical Multiplexed Board (OMB) [7], able to analyze two fibres, both of then carrying the same data, and provide the correct one to the ROD input.

The interest of this project was initially raised in February 2003. At that time a solution was proposed for the OMB based on exhaustive on-line analysis of the data carried by both of the fibres using FPGAs for implementation. That architecture was called "MiniROD" as it followed a ROD-like design.

The Universidad de Valencia – IFIC (Spain) collaboration showed interest to develop this project, to study its technical viability and to make a first prototype. In particular, the main goals were:

- To implement fiberoptic switching to take advantage of redundancy.
- To obtain real (production) costs.
- To design a software and hardware development platform.
- To try different alternatives for data error analysis (CRC, etc.).

The OMB was also thought to work in a "Data Injector Mode" where data patterns could be injected into the ROD motherboard for test and verification purposes.

The project started in October 2003 and a first OMB prototype is now finished. The Optical Multiplexer Board prototype has been designed in a 6U VME64x slave module architecture. It includes four optical inputs connectors (two input channels) and two optical outputs connectors integrated in the PCB. The input channels are capable to read up to 4x16 bits at 40 MHz and allow testing different input technologies. The output also runs at 40 MHz with a data width of 16 bits.

There are also four input G-Link chips on the board, two output G-Link chips, two CRC FPGAs and one VME FPGA. These lasts are implemented on ALTERA devices. Furthermore, for the Data Injector Mode, the OMB has two additional copper input cables: Trigger and Busy. These external signals are included in this prototype to send correctly internal data in order to test the ROD functionality.

Apart from selecting the error free input fiber for each channel, the module has been provided with an Injector Mode operation to mimic the TileCal FEB to test the ROD.

The layout of the board is shown in Fig. 6. A short description of the main functions of the G-link and FPGA chips in the OMB board is given in Table 1.

The main description for the OMB is:

A. Input Description:

Four optical fibers coming from the FEBs are the input to the OMB, and two optical fibers to the ROD are the output from the OMB.

The G-link chip (HDMP-1034) is used in the input stage of the OMB board. The serializer (HDMP-1032) is used in the output stage of the OMB board. The HDMP-1032 transmitter and the HDMP-1034 receiver chips are used to build a high-speed data link for point-to-point communication. They are monolithic silicon bipolar chips.

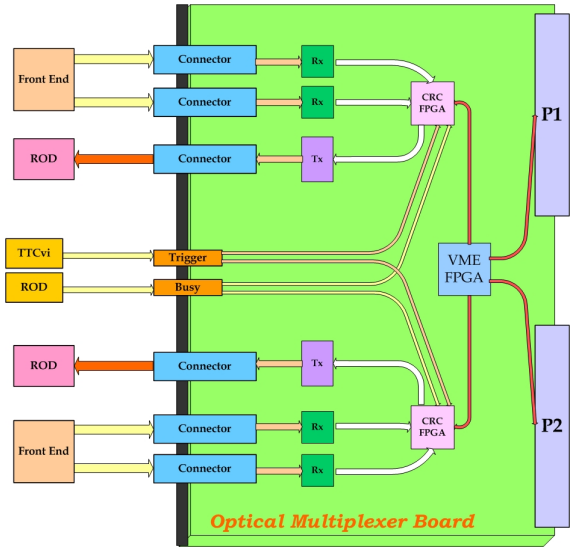

Fig. 6. Optical Multiplexer Board Block Diagram.

TABLE I
OMB Main Components

Component	Main Function	Chip
6 G-Link Chips	Deserialize the incoming data. Serialize the output data.	HDMP-1034 HDMP-1032
2 CRC FPGAs	Send correct data to ROD. ROD Injector Data.	CYCLONE EP1C12
1 VME FPGA	Interfaces OMB to VME.	ACEX EP1K100

Parallel data loaded into the transmitter chip is delivered to the receiver chip over an optical fiber, and is reconstructed into its original parallel form. The HDMP-1032/1034 chipset handles all the issues of link startup, maintenance and simple error detection. It transmits 16 bits of parallel data in dual-frame mode.

B. CRC FPGA Description:

Two CRC FPGA CYCLONE EP1C12 are used in the OMB board. The main reason for the choice these chips is the low cost of this FPGA. The incoming data from two different G-link receiver chips is routed to one CRC FPGA. The different and redundant incoming data are analyzed and CRC FPGA decides which the correct data link is. The CRC FPGA routes the correct data to one G-link transmitter chip.

C. VME Interface of OMB:

The OMB module is considered a VME slave module. All actions and commands are controlled by the crate CPU and the communication follows the VME64 standard. The VME interface of the OMB is implemented in an ACEX EP1K100, the VME FPGA.

VME map includes registers holding the number of CRC errors detected in the optical fibers, control registers to select CRC checking or injection mode and a event memory to load the data to inject if we use this mode. The addressing mode is A32D32 and the memory space also includes a CR/CSR space to conform to CERN specifications in this aspect.

The VME FPGA exchanges data between the VME CPU and the two CRC FPGAs. Fig. 7 shows the OMB memory map.

	PREROD VME MEMORY MAP (A32 ACCESS)	
OFFSET	**DESCRIPTION**	**TYPE**
0x00	BASE REGISTER	R/W
0x04	STATUS/CONTROL REGISTER	
0x10	**LINK A CH1** CRC16 ODD ERRORS	R
0x14	**LINK A CH1** CRC16 EVEN ERRORS	R
0x18	**LINK A CH1** CCITT-CRC16 ERRORS	R
0x1C	**LINK A CH2** CRC16 ODD ERRORS	R
0x20	**LINK A CH2** CRC16 EVEN ERRORS	R
0x24	**LINK A CH2** CCITT-CRC16 ERRORS	R
0x30	**LINK B CH1** CRC16 ODD ERRORS	R
0x34	**LINK B CH1** CRC16 EVEN ERRORS	R
0x38	**LINK B CH1**CCITT-CRC16 ERRORS	R
0x3C	**LINK B CH2** CRC16 ODD ERRORS	R
0x40	**LINK B CH2** CRC16 EVEN ERRORS	R
0x44	**LINK B CH2** CCITT-CRC16 ERRORS	R
0x50	**LINK A VME** TRIGGER FREQUENCY DIVIDER	R/W
0x54	**LINK B VME** TRIGGER FREQUENCY DIVIDER	R/W
0x58	LOOP LIMIT LINK A (VME TRIGGER)	R/W
0x5C	LOOP LIMIT LINK B (VME TRIGGER)	R/W
0x100-0X1FF	INJECTION EVENT MEMORY	R/W

Fig. 7. VME memory map of the Optical Multiplexer Board

D. Data Distribution in OMB:

There are two different function modes in OMB, CRC process mode and ROD Injector Data mode. In the first, data coming from the Front End is analyzed running a CRC algorithm in real time. If errors are detected, the data from the other fiber is sent to ROD. In the ROD Injector Mode internally generated or preloaded data is sent to ROD motherboard. In this last one, G-Link receivers are not used.

E. Power Distribution in OMB:

There are two ways of applying the main power supply (3.3V) in the OMB board:

- From the VME backplane 3.3V pins.
- From the VME backplane 5V pins and ulterior conversion that into 3.3V with a DC/DC converter (PT5801).

The +5V from the VME back plane is used by the trigger/busy logic and is also used to obtain +2.5V necessary for VME FPGA. ADP3330-2.5 is the DC/DC converter used to obtain this voltage.

The +12V, -12V and -5V from the VME back plane is used by the trigger/busy logic too.

IV. Signal Integrity Issues in the Optical Multiplexer Board Design

On of the main aspects we cared about in the designing of this board was signal integrity. Even if the clock frequency used is not that high (40 MHz) it is true that we faced several 32-bit buses to be routed, so crosstalk might be something to worry about.

We carried signal integrity studies both in pre-layout and post-layout stages using Cadence SpecctraQuest software. Pre-layout analysis let us to establish the routing rules and the chose of termination resistor if needed. Post-layout analysis verified the design taking into account the PCB layer organization.

As an example, the differential lines connecting the fiberoptic transceivers and the HDMP chips at 640 Mbps were studied in a pre-layout phase. In this case we established the equal routing length and let the software simulate the behaviour with different termination resistors. Fig. 8 shows the topology for this case.

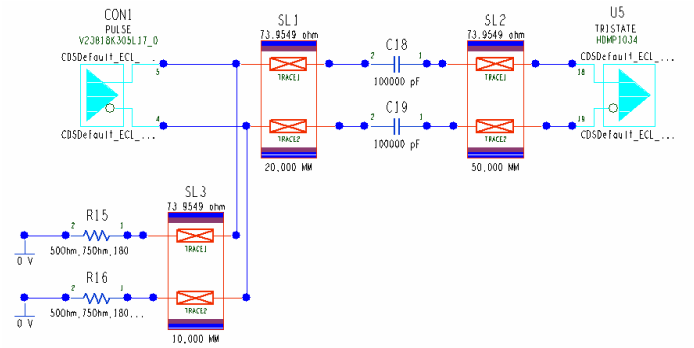

Fig. 8. Differential lines topology from optical fiber connector to HDMP.

The results of the simulation for different resistor values are shown in Fig. 9. From them a 180 ohm value has chosen as termination.

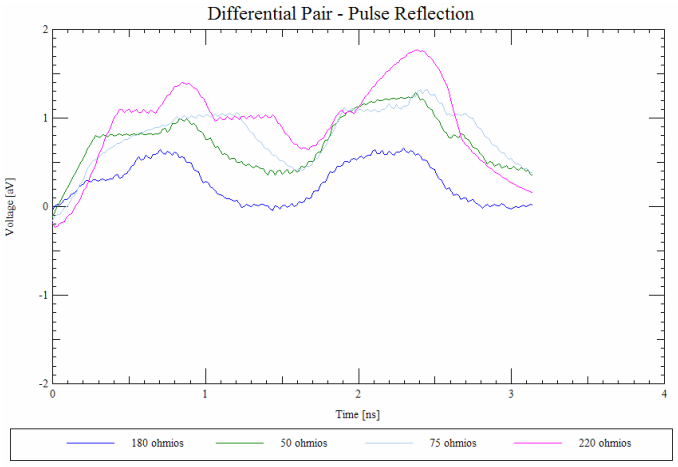

Fig. 9. Received pulse at the HDMP input for different terminations.

Another important issue in high speed digital design is clock distribution. In our case we had the option to mount just one clock for all the HDMP's as we used one clock for each FPGA. This option is very sensitive to trace distance and would imply strict routing rules which may lead (as we were very space limited) to an impossible solution. Besides, taking into account that input and output optical link need not to be synchronized among them we preferred to used one clock device for each HDMP. Pre-layout simulations helped in this decision as the option with only one clock chip performed worse than the multiple clock one. Fig. 10 shows the simulations for 1 clock and multiple clocks.

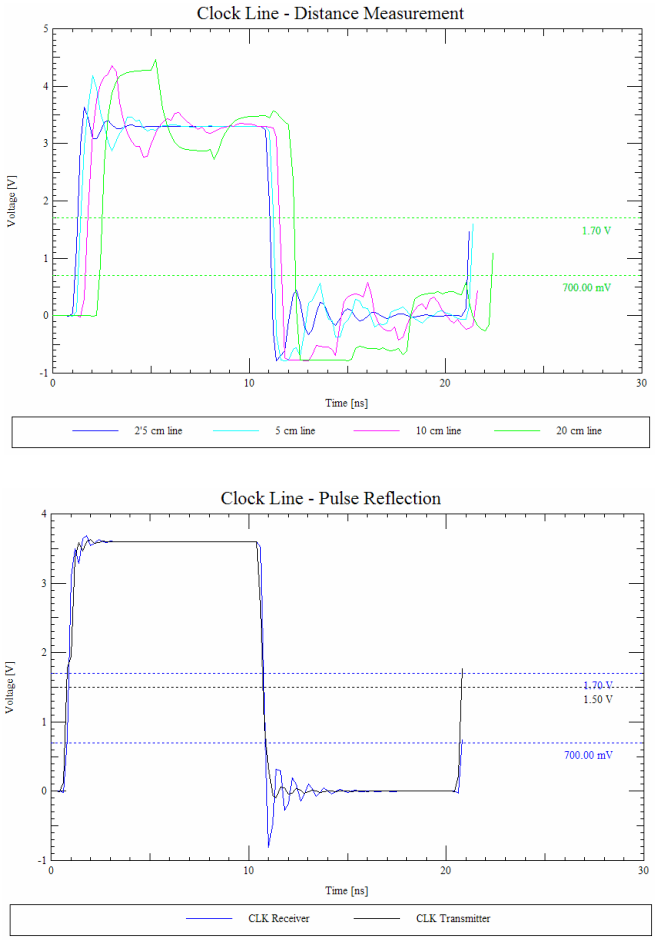

Fig. 10. Clock line reflection simulations for (a) one and (b) multiple clocks

V. Optical Multiplexer Board Tests

In July-August 2004, first tests were carried out on the OMB prototype at CERN (Fig. 11). These tests were intended to provide an overall look and debug its functionalities.

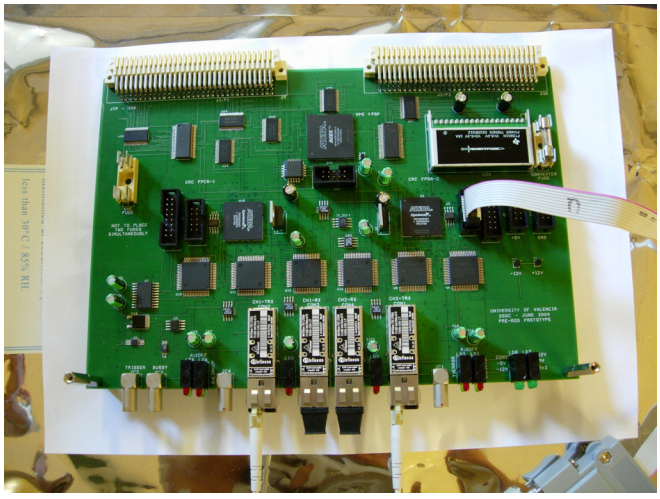

Fig. 11. Optical Multiplexer Board.

Basic electrical tests were already performed at Valencia labs while at CERN the test were related with the input/output data flow (Fig. 12). For this purpose we used a custom data injector PCB to simulate data coming from the detector and a ROD motherboard as data receiver for the output fibres of the OMB. To test the Data Injector Mode, the OMB directly output data to the ROD motherboard.

With the data acquisition software developed for the ROD motherboard control (described in section III) it was possible to check for data corruption or transmission errors.

OMB modules have been used in precomissioning phase of the TileCal ROD motherboards at Valencia lab and also at USA15 at CERN from last weeks of September 2005. The module has shown a perfect stability. Fig 13 shows a picture of the installation at USA15.

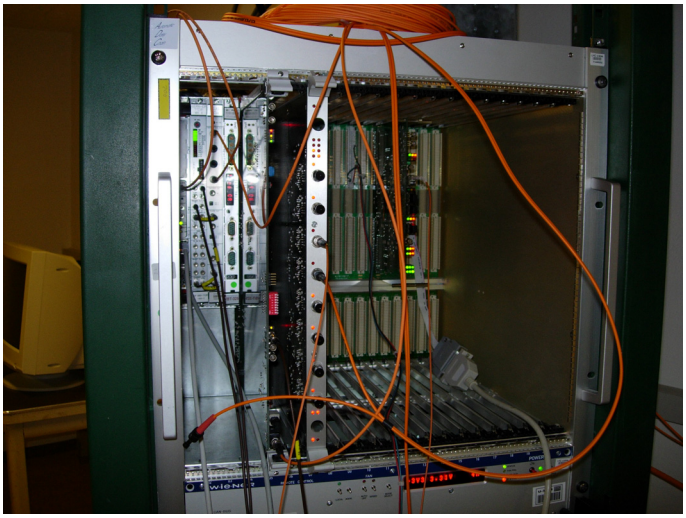

Fig. 12. OMB test setup at CERN laboratories.

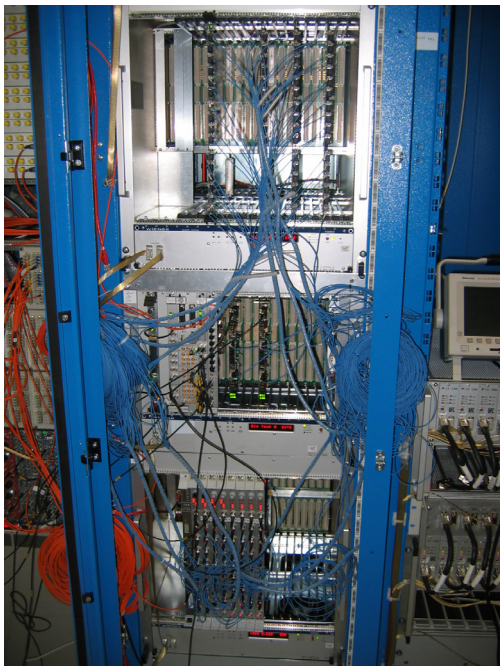

Fig 13. Pre commissioning test at USA15

VI. Summary and Future Work

This paper has presented the current status of development of the TileCal ROD system. This system consists, speaking of new electronic designs, of a ROD motherboard and an Optical multiplexer board. The design of the second one is a completely new design. In what respects to the OMB, after the results of the tests, the board is now undergoing a redesigning phase which includes the adoption of the final 9U board size, 8 inputs channels (16 input fibres) and 8 output channels, as well as TTC signal decoding and VME full control. We expect to have a preproduction board series by winter 2005.

In the overall, a TileCal ROD system has proven all its functionalities and foresees the fulfilment of all requirement of the TileCal schedule.

References

[1] ATLAS Trigger and DAQ steering group, "Trigger and DAQ Interfaces with FE systems: Requirement document. Version 2.0", *DAQ-NO-103*, 1998.

[2] J. Dowell, M. Pearce, "ATLAS front-end read-out link requirements", *ATLAS internal note, ATLAS-ELEC-1*, July 1998.

[3] J. Castelo, "TileCal ROD HW Requirements and LArg compatibility", Reference: http://ific.uv.es/tical/rod/doc/ROD_tical_HW.pdf.

[4] O. Boyle, R. McLaren, E. van der Bij, "The SLINK interface specification", *ECP Division CERN*, March 1997.

[5] J. Torres, E. Sanchis, J. Castelo, V. González, G. Torralba, J. Martos, "On the developments of the Read Out Driver for the ATLAS Tile Calorimeter", *7th Workshop on Electronics for LHC Experiments*, Stockholm 2001.

[6] J. Torres, J. Castelo, E. Fullana, "ROD General Requirements and Present Hardware Solution for the ATLAS Tile Calorimeter", *8th Workshop on Electronics for LHC Experiments*, Colmar 2002.

[7] J. Torres et al., "Optical Multiplexer Board for TileCal Data Redundancy", *9th Workshop on Electronics for LHC Experiments*, Boston 2004.

[8] F. Camarena, J. Castelo, E. Fullana, "Optimal Filtering applied to 1998 Test Beam of Module 0", *ATL-TILECAL-2002-015*, 2000.