Xilinx® Spartan™-3 Development Kit

Table of Contents

Figures

Tables

1.0 Introduction

The purpose of this manual is to describe the functionality and contents of the Xilinx Spartan-3 Development Kit from Avnet Design Services. This document includes instructions for operating the board, descriptions of the hardware features and explanations of the example projects.

1.1 Description

The Spartan 3 Development Kit provides a platform for engineers designing with the Xilinx Spartan 3 FPGA. The board provides the necessary hardware to not only evaluate the features of the Spartan 3 but also to implement complete user applications. Example projects are provided to help the user understand the design tool flow of the Xilinx Embedded Development Kit (EDK) software environment.

1.2 Features

- FPGA
  - Xilinx XC3S1500/2000-FG676 Spartan-3 FPGA
- I/O Peripherals
  - 2x16 character LCD
  - 128x64 OSRAM OLED graphical display
  - DB15 & video DAC
  - Audio CODEC
  - PS2 keyboard & mouse ports
  - 8-position DIP switch
  - 2 push-buttons
  - 8 discrete LEDs
  - Piezo buzzer
  - 3, 140-pin general purpose I/O expansion connectors (AvBus)
  - Up to 30 LVDS pairs
  - 1, 50-pin 0.1" header for easy I/O access
- Memory
  - Micron DDR SDRAM (32 MB)
  - 16 MB FLASH
  - 2 MB SRAM
- Communication
  - RS-232 serial port
  - 10/100 Ethernet
  - USB 2.0
- Configuration
  - Xilinx platform FLASH configuration PROM(s)
  - Parallel IV cable support for JTAG
  - Fly-wire support for Parallel III and MultiLINX™

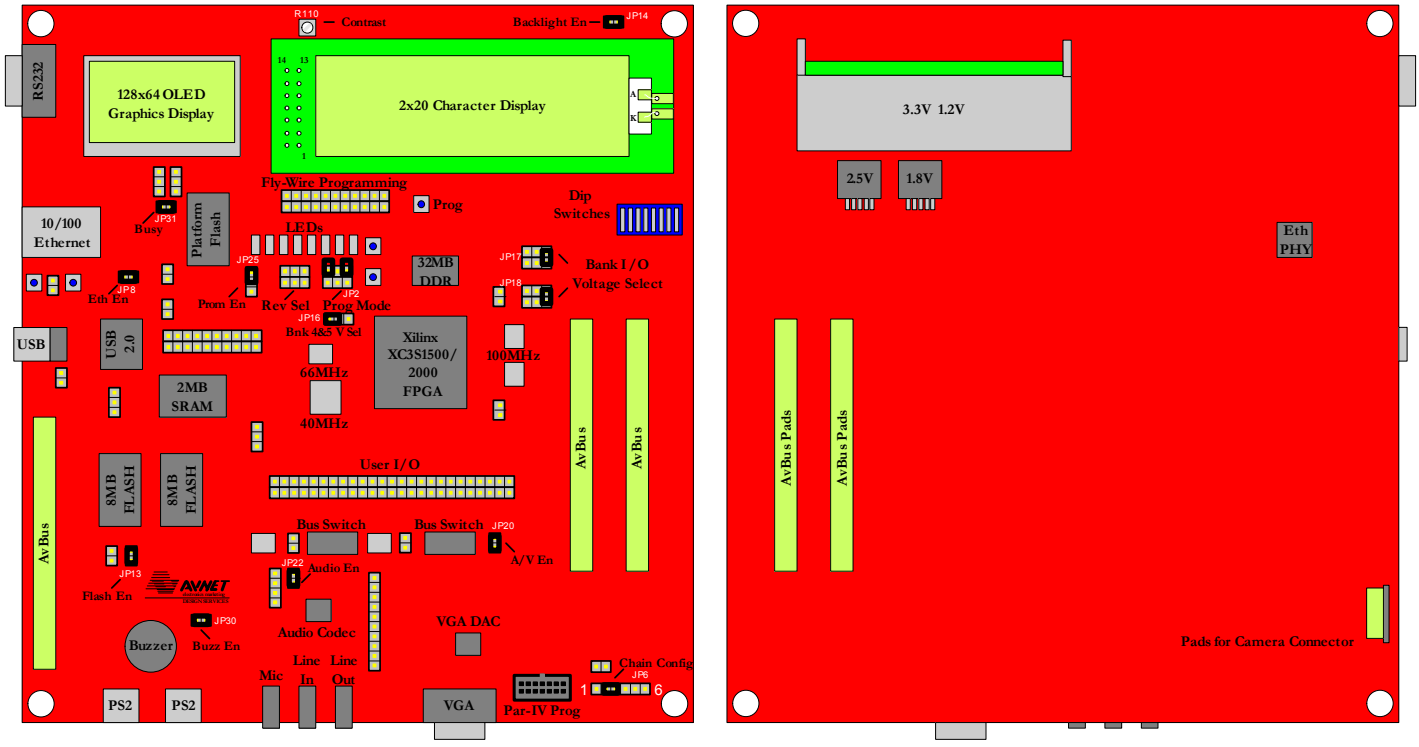


Figure 1 - Spartan-3 Dev (Top Side)

Figure 2 - Spartan-3 Dev (Bottom Side)

1.3 Demo Applications

The Spartan-3 Development Kit from Avnet Design Services comes with example projects designed in Xilinx Platform Studio (XPS). XPS is a software tool in the Xilinx Embedded Development Kit that provides the user with a single tool flow for creating both hardware and software systems. The example projects help the user to more quickly learn the XPS tool and develop user-specific applications by leveraging already tested and functional designs. The example projects that will be discussed in detail later in this document are listed below.

*Note: For additional demo applications, please contact your local Avnet FAE.

- Hello World Project
- External Memory Project(s)
  - An OPB_DDR SDRAM memory project uses the MicroBlaze for accessing on-board DDR SDRAM.
  - An OPB_EMC project uses the MicroBlaze for accessing on-board SRAM and Flash memory.
  - Using the MicroBlaze soft processor, execute code from internal Block RAM or external memory.
  - Use the JTAG debug interface to download modified executable files to internal or external memories.
- Ethernet Web Server
  - MicroBlaze system uses the OPB_EMAC to serve up web pages.
  - Uses on-board 10/100 National PHY

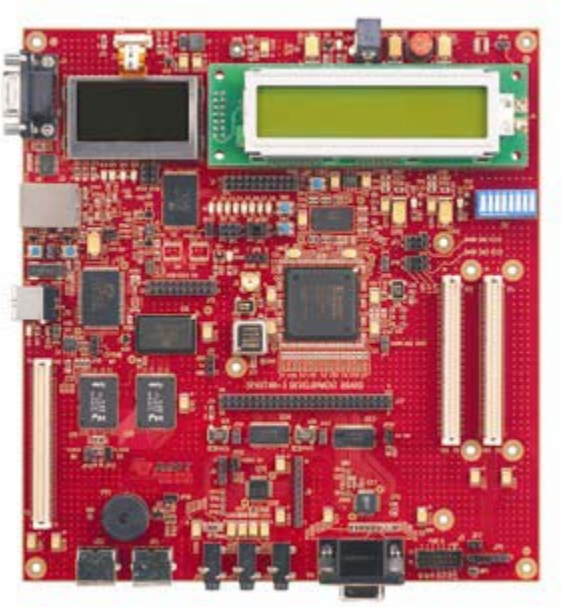


Figure 3 - Spartan-3 Development Board Picture

1.4 Ordering Information:

The following table lists the evaluation kit part numbers and available software options.
Internet link at http://www.em.avnet.com/ads or www.em.avnet.com/spartan3dev

Part Number	Hardware
ADS-XLX-SP3-DEV1500	Spartan-3 Development Kit with an XC3S1500
ADS-XLX-SP3-DEV2000	Spartan-3 Development Kit with an XC3S2000

Table 1: Ordering Information

2.0 Hardware

This section of the manual describes the hardware of the Spartan-3 Development board. The hardware was designed with the Spartan-3 FPGA as the focal point. The block diagram is shown in Figure 4.

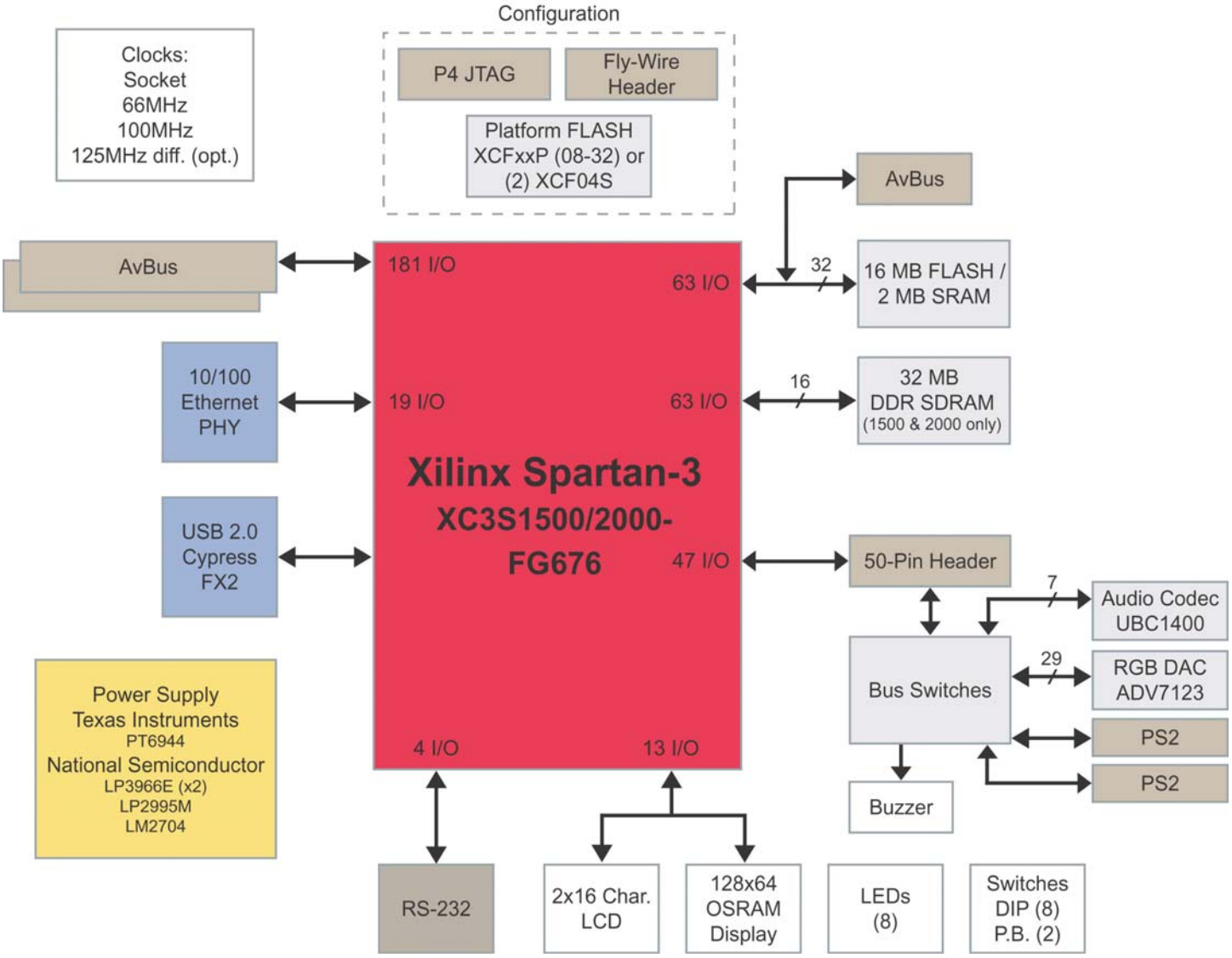


Figure 4 - Spartan-3 Development Board Block Diagram

2.1 Spartan-3 FPGA

The Spartan-3 Development board was designed to support the Spartan-3 FPGA in the 676-pin, BGA package (FG676). The FG676 package supports three mid-range densities (1000, 1500, and 2000). The board was designed to support two of the three densities: the 3S1500 and 3S2000. The schematic symbol used for the Spartan-3 device indicates the specific I/O pins available in each density (396 I/Os with 2VP7 and 556 I/Os with the 2VP20/30). Table 3 describes the attributes of the Spartan-3 device based on density.

Spartan-3 Part	System Gates	Logic Cells	CLB Array (One CLB=Four Slices)			BlockRAM (bits)	BRAM	Dedicated Multipliers	DCMs	Max User I/O
			Rows	Col	Total CLBs					
XC3S1500	1.5M	29,952	64	52	3,328	576K	32	32	4	
XC3S2000	2M	46,080	80	64	5,120	720K	40	40	4	

Table 2 - Spartan-3 Attributes by Density

2.2 Configuration

The Spartan-3 Development board supports Boundary-scan as well as Master/Slave Serial and Master/Slave Parallel (SelectMAP) using the on-board PROMs. All configuration pins are brought out to "J1", should the user wish to program with an alternate method.

2.2.1 Boundary scan

Programming the Spartan-3 FPGA via Boundary-scan requires a JTAG download cable (not included in the kit). The Spartan-3 Development board has connectors to support both the flying leads connection of the Parallel Cable III and the ribbon cable connection of the Parallel Cable IV. These connectors are labeled "J1" and "J5" respectively.

The FPGA and Platform Flash are both in the JTAG chain and both may be configured via the chain. When programming the FPGA via the JTAG interface, it is good practice to place the device in Boundary Scan mode. This may be accomplished using the Mode select jumpers at JP2. The jumper positions are labeled M0 – M2 and are all LOW by default. So placing a jumper provides a HIGH. The Spartan-3 FPGA is set to Master Serial mode when no jumpers are installed on JP2. To set the FPGA to boundary-scan mode, install shunts on JP2 at locations 1-2 & 5-6 as shown in below. Note that power should be removed when changing Mode select jumpers.

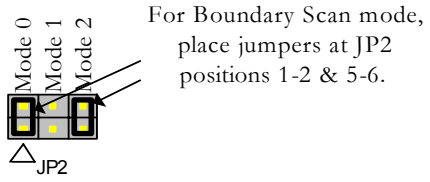


Figure 5 – Boundary Scan Mode Selection via JP2

JTAG Header (J1)

J1 is a standard 0.1" header and is intended for use with flying leads, such as those of the Xilinx Parallel Cable 3 (PC3) downloading/debugging cable. Connect the leads as indicated below for "J1".

Signal Name	Par-3 (J1) pin	PAR-4 Ribbon (JP6) pin
VCC	20	2
TDI	9	10
TDO	15	8
TMS	13	4
TCK	11	6
GND	19, 21	1,3,5,7,9,11 or 13

Table 3 - JTAG Headers (Par-3 & Par-4) Pin-Out

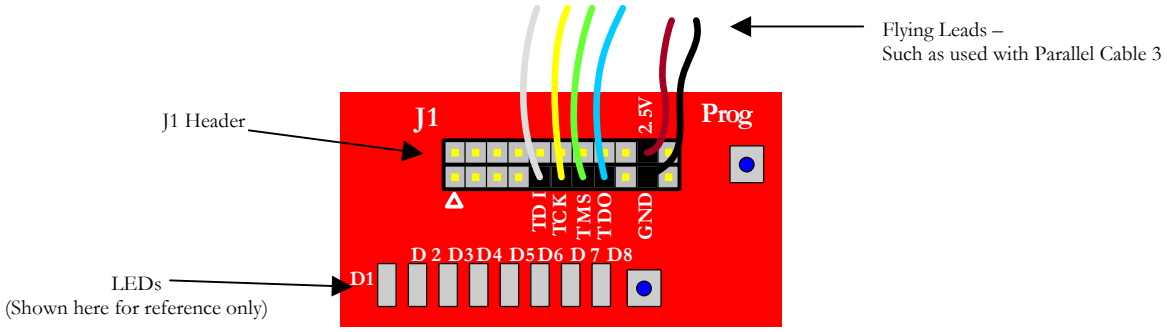


Figure 6 - Configuration / Debug Connections – Par3

Parallel Cable IV / MultiPro Ribbon (J5)

J5 is intended for connection to a 14-pin ribbon as supplied with a Xilinx Parallel Cable IV or MultiPro Desktop Tool. Connect the ribbon cable to JP6 as shown below. Note that the ribbon and connector are keyed to ensure proper connection.

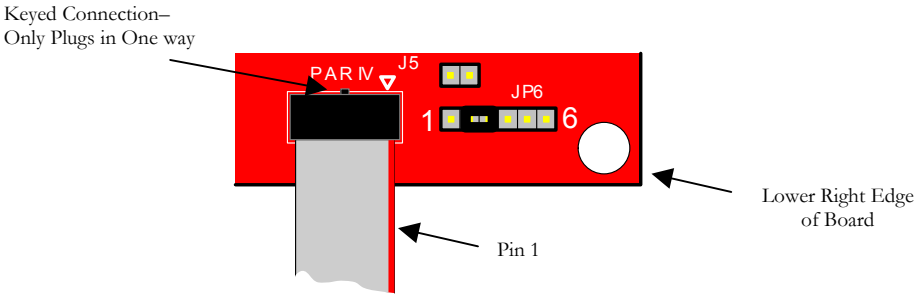


Figure 7 - Configuration / Debug Connections – Par IV

For further information regarding Xilinx configuration solutions, please visit:
http://www.xilinx.com/products/design_resources/config_sol/index.htm

Modifying the JTAG Chain

By default, the Spartan 3 Development board JTAG chain includes a Platform Flash and the FPGA. The board provides the user with the ability to add/remove devices from the JTAG chain. Each device may be bypassed by way of 0 ohm resistor jumpers. The header labeled "JP6" allows the user even more flexibility with the chain. By moving this jumper, you may add in the chains of daughter-boards by way of the AvBus. Most users, however, will only use the JTAG chain in standalone mode (default) with a jumper installed across pins 2-3 on JP6. It is recommended to start with this mode and review the schematic carefully if you wish to change it.

"JP7" JTAG Chain Selection – Jumper Settings	
Pins 2-3	**Standalone Mode** – Spartan-3 and XC18V04 PROMs
Pins 1-2 and 4-5	Add AvBus P1 Connector to standalone

Table 4 - JTAG Chain Selection "JP6"

PROM FPGA

Default
Chain

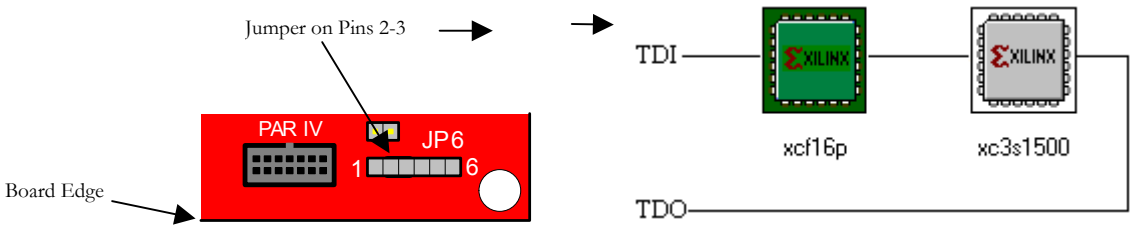


Figure 8 - JTAG Chain Standalone Mode (Default)

2.2.2 Configuration With Platform Flash

The Platform Flash PROM(s) provide easy-to-use non-volatile storage for the configuration file. These devices are in–system programmable via the boundary scan chain and may program the FPGA in Master Serial, Master SelectMAP, Slave Serial, or Slave SelectMAP modes. After programming the proms with configuration data, remove power and set JP2 appropriately as indicated below. When power is re-applied, the FPGA will clock data from the PROMs using the selected mode.

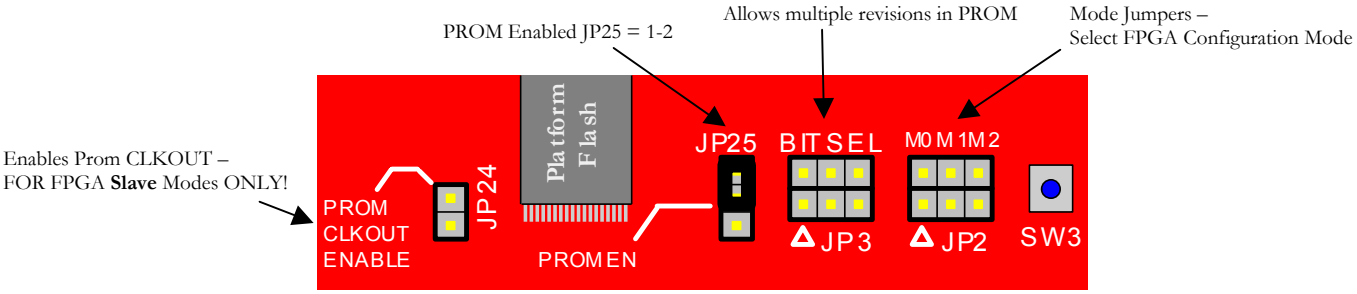


Figure 9 – Design Revision "BIT SEL" Jumpers JP3

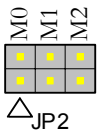
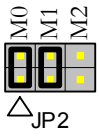
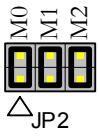
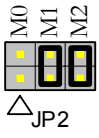
Configuration Mode (M0 : M1 : M2)	Prom Clock En JP24	Prom Enable JP25	Mode Jumpers JP2	Notes
Master Serial **DEFAULT** (0:0:0)	 JP24	 JP25	 JP2	**DEFAULT** FPGA provides CCLK
Master Parallel (Master SelectMAP) (1:1:0)	 JP24	 JP25	 JP2	FPGA provides CCLK
Slave Serial (1:1:1)	 JP24	 JP25	 JP2	PROM provides CCLK
Slave Parallel (Slave SelectMAP) (0:1:1)	 JP24	 JP25	 JP2	PROM provides CCLK

Table 5 – FPGA Configuration from PROM … Jumper Setting

Design Revisioning With Platform Flash

The Spartan-3 Development Board is designed to support the advanced features of the parallel Platform Flash PROM including support for multiple design revisions and compressed configuration files. These features are disabled by the default jumper settings. If an MCS (prom file) has been built with multiple revisions, use the "BIT SEL" jumper (JP3) to select the desired revision. By default, no jumpers are installed and rev 0 will be loaded. To load revision 1, a jumper would be placed at JP3 position 1-2.

2.2.3 Custom Configuration Methods

In addition to JTAG chain signals, J1 provides the user with an interface to the FPGA dedicated and dual function programming pins. This enables fly-wire support for the programming methods mentioned above and gives flexibility for developing a custom programming solution.

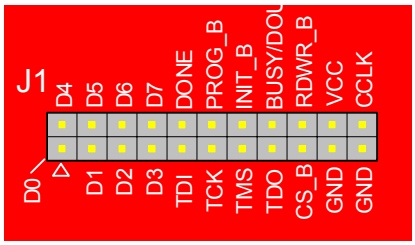


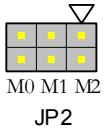
Figure 10 - Fly Wire Connection J1

2.3 Jumper Settings

This section provides a description of the jumper settings for the Development board. The jumpers are listed in order by JP number. The board is ready to use out of the box with the default jumper settings.

JP1 "BNK 2&3 VRef" – Supplies a 1.25V reference voltage to the VREF inputs of banks 2 & 3. Use only if your I/O standard requires a reference voltage of 1.25V. Note that when installed, all VREF pins in banks 2 & 3 will be connected to the 1.25V reference rail. Any unused reference pins should be dealt with appropriately, or the FPGA may have an adverse affect on the rail. One option for unused VREF pins is to use the config prohibit attribute in the UCF and then use tri-state option for unused I/O in bitgen. Another option may be to use "dummy" inputs to ensure the FPGA will not drive the unused VREFs.
Default: Uninstalled; BNK 2&3 Vref not connected to 1.25V rail.

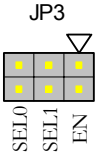
JP2 "MODE SELECT" – Configuration mode selection. Use to select the configuration mode for the FPGA. With no jumpers installed, these pins are pulled low enabling Master Serial mode. Installing jumpers on JP2 will pull the corresponding mode pin high, as indicated in the Figure below. See the Configuration section of this document for further information.
Default: Uninstalled; Master Serial mode; FPGA will be configured from Platform Flash.



JP2 Config Mode	1-2 M0	3-4 M1	5-6 M2
Master Serial	0	0	0
Slave Serial	1	1	1
Master SelectMAP	1	1	0
Slave SelectMAP	0	1	1
Boundary Scan	1	0	1

Figure 11 - FPGA Configuration Mode Select

JP3 "Bit Select" – Design Revision Select, selects the configuration design when the PROM is programmed with multiple revisions. When no jumpers are installed, the PROM is set for external selection mode with revision 0 selected. Installing jumpers on JP3 will pull the corresponding select pin high, as indicated in the Figure below.
Default: Uninstalled; external enabled using Rev0



JP3 Revision Select	1-2	3-4	5-6
External disabled	x	x	1
Enabled – Rev. 0	0	0	0
Enabled – Rev. 1	1	0	0
Enabled – Rev. 2	0	1	0
Enabled – Rev. 3	1	1	0

Figure 12 - Design Revision Select

JP4 "HSWAP_EN" – Enables pull-ups on the Spartan-3 I/O pins during configuration. A pull-down resistor is used to enable the I/O pull-ups during configuration. Install a jumper to disable the configuration pull-ups.
Default: Open; pull-ups enabled.

JP6 – JTAG chain configuration. Selects the JTAG chain configuration. Install a jumper across pins 2-3 for standalone mode. Install jumpers across pins 1-2 and pins 4-5 to add the AvBus connector labeled "P1" to the standalone chain. These settings are described in the Hardware section of this manual (see "Modifying the JTAG Chain" in **Boundary scan** section).
Default: Installed across pins 2-3; standalone chain mode.

JP7 – JTAG TRST#, forces TRST low.
Default: Open, pulled-high.

JP8 "ETH EN" – Ethernet Enable, connects an I/O pin on the FPGA to the reset pin of the Ethernet PHY. See the "PHY_RST#" net on the schematic. The PHY is held in reset by a pull-down resistor when a jumper is not installed.
Default: Installed, FPGA drives the PHY reset.

JP9 "USB 5V" – USB 5.0V Power, when installed allows the USB host to supply the 5.0V rail of the evaluation board over the USB connection. This is not recommended since the evaluation board requires more current than USB specification provides for. Using the USB port for board power may damage the USB host (the PC or laptop).
Default: Open, board power comes from J7 connector.

JP10 "USB EEPROM WC#" – Serial EEPROM write protect, install a shunt to protect programmed data.
Default: Open, read/write enabled.

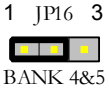
JP11 "USB DIS" – USB Disable, install a shunt to hold the Cypress EZ-USB device in reset. When open, the USB reset line is controlled by either an I/O pin of the FPGA or the push-button labeled "SW2".
Default: Open, the FPGA or push-button controls the USB reset.

JP12 "FLASH WP#" – Flash write protect. When jumper is installed, WP# will be tied hard low. When uninstalled, WP# is pulled high via pull-up resistor.
Default: Uninstalled; write protect not active.

JP13 "FLASH RESET" – Connects the flash reset pin to the FPGA. This connection is only available on the 2000 density part. When uninstalled (or unavailable ie...1500 density part), the flash reset will be inactive (flash enabled) by way of resistor pull-up on the board.
Default: Installed

JP14 "LCD BACKLIGHT" – Enables the LED backlight panel on the 2x20 LCD.
Default: Installed

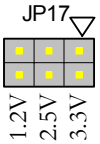
JP16 "BANK 4&5 VCCO VOLTAGE" – VIO Selection, selects the I/O voltage for FPGA banks 4 and 5. Only one jumper should be placed at this connector. Valid placements are 1-2, 2-3 as indicated in the Figure below.
Default: Installed across pins 1-2; 3.3V supply.



Jumper Position	1-2	2-3
I/O Voltage	3.3V	2.5V

Figure 13 - I/O Voltage Selection Banks 4&5

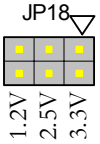
JP17 "BANK 0&1 VCCO VOLTAGE" – VIO Selection, selects the I/O voltage for FPGA banks 0 and 1. Only one jumper should be placed at this connector. Valid placements are 1-2, 3-4, or 5-6 as indicated in the Figure below.
Default: Installed across pins 1-2; 3.3V supply.



Jumper Position	1-2	3-4	5-6
I/O Voltage	3.3V	2.5V	1.8V

Figure 14 - I/O Voltage Selection Banks 1&2

JP18 "BANK 2&3 VCCO VOLTAGE" – VIO Selection, selects the I/O voltage for FPGA banks 2 and 3. Only one jumper should be placed at this connector. Valid placements are 1-2, 3-4, or 5-6 as indicated in the Figure below.
Default: Installed across pins 1-2; 3.3V supply.



Jumper Position	1-2	3-4	5-6
I/O Voltage	3.3V	2.5V	1.8V

Figure 15 - I/O Voltage Selection Banks 2&3

JP20 "A/V ENABLE" – The Video DAC, Audio Codec, PS2 Ports, and Buzzer are connected to the FPGA by way of bus switches. Installing this jumper will enable the switches, thereby connecting the peripherals to the FPGA. Removing this jumper will disable the switches, disconnecting the peripherals from the FPGA. This may be desirable if the 50-pin I/O header is to be used instead of the A/V peripherals.
Default: Installed; A/V peripherals enabled.

JP21 "CODEC CLK DISABLE" – Installing this jumper will disable the 24.576MHz oscillator to the Codec.
Default: Uninstalled, codec oscillator enabled

JP22 "AUDIO EN" – When uninstalled, the Codec is held in reset by a resistor pull-down. When installed, the reset line is connected to the FPGA, allowing it to take the codec out of reset.
Default: Installed, FPGA controls reset line.

JP23 "VIDEO CLK DISABLE" – Installing this jumper will disable the 25.175MHz oscillator to the video DAC.
Default: Uninstalled, DAC oscillator enabled

JP24 "PROM CLKOUT ENABLE" – When installed, Enables the prom clkout to drive the configuration clock (CCLK) for FPGA Slave Mode configuration. If using the PROM device as the clock source, make sure the jumper on JP27 is not installed and that the jumper settings on JP2 put the FPGA in a Slave configuration mode. Note: The PROM must supply CCLK when a compressed configuration file is used.
Default: Open, the FPGA provides the configuration clock.

JP25 "PROM ENABLE" – PROM Enable, position 1-2 connects the DONE pin on the FPGA to the chip enable pin of the PROM(s). Position 2-3 will pull the enable low. The PROM is disabled by a pull-up resistor when a jumper is not installed.
Default: Installed on 1-2; using the DONE pin, the PROM is enabled when the FPGA is not configured.

JP27 "USB CCLK ENABLE" – USB CCLK Enable, when installed enables the USB device to drive the configuration clock of the FPGA. If using the USB device as the clock source, disable the PROM by removing the jumper on JP25 and make sure the jumper settings on JP2 put the FPGA in a Slave configuration mode.
Default: Open, the FPGA or PROM provides the configuration clock.

JP28 "USB RS232 RX" – This signal is intended to be an output from the FPGA to either the RX Input of the EZUSB chip or the TXIN2 of the RS232 IC. Jumper on 2-3 connects the USB RX signal to the FPGA. Jumper on 1-2 connects RS232 signal TX2 to the FPGA.
Default: none; neither signal connected to the FPGA

JP29 "USB RS232 TX" – This signal is intended to be an input to the FPGA from either the TX output of the EZUSB chip or the RXOUT2 of the RS232 IC. Jumper on 2-3 connects the USB TX signal to the FPGA. Jumper on 1-2 connects RS232 signal RX2 to the FPGA.
Default: none; neither signal connected to the FPGA.

JP30 "Buzz Enable" – Connects "buzzer" net. Remove this jumper to disable the piezo buzzer.
Default: Installed, buzzer enabled.

JP31 "Prom Busy" – Connects net "prom_busy" to net "fpga_busy". Support for a PROM errata which will likely be obsolete by the time this document is published.
Default: Installed

The following figure illustrates the default placement of the jumpers installed on the Spartan-3 Development Board.

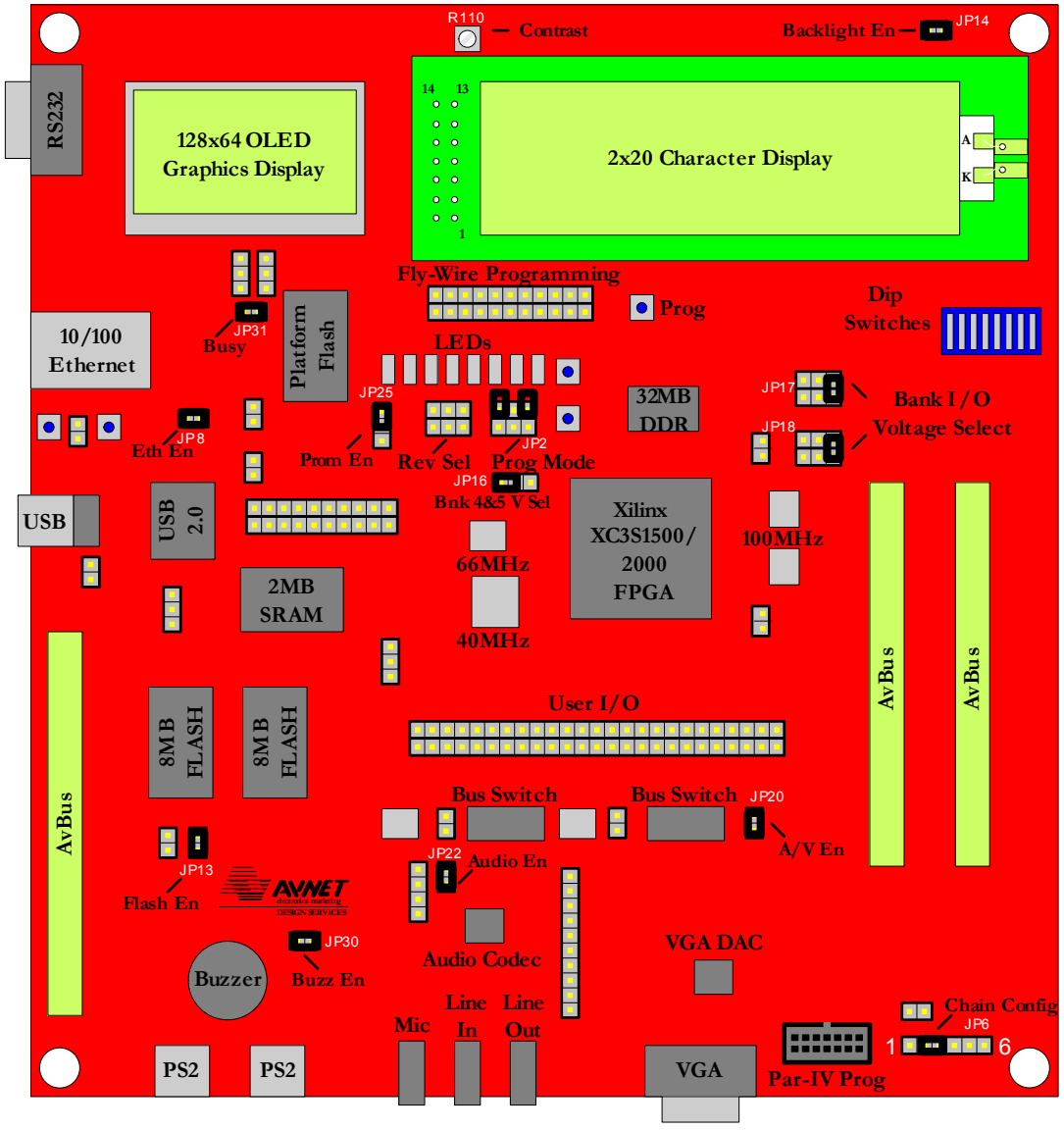


Figure 16 - Default Jumper Placement

JTx Resistor Jumpers –
Additional flexibility has been designed into the circuit in the form of resistor jumpers "JTx" and series resistors that can be moved or removed to alter the functionality of the board. The purpose of some of these components may be discussed in other sections of this manual others may not be discussed at all. The position of these components should not be altered without careful review of the schematics and associated component data sheets to prevent damage to the board.

2.4 Clocks

The available clock sources on the Spartan-3 Development board are shown below. The following were brought in on global clock inputs and are recommended for use as system clocks.

- Single-ended, 66MHz Oscillator – FPGA pin "AD13"
- Single-ended, 100MHz Oscillator – FPGA pin "A13"
- Single-ended socket, 40MHz Oscillator – FPGA pin "AE14"
- Single-ended SMA input – FPGA pin "AE13"
- Single-ended header input – FPGA pin "AF14"
- Differential, Optional Oscillator Pads (U14) – FPGA pins "C14" (P) and "B14" (N)

Freq	GCLK Input	FPGA pin#	Notes
66MHz	YES	AD13	
100MHz	YES	A13	
40MHz typ.	YES	AE14	Socket
-	YES	AE13	SMA
-	YES	AF14	Header
125MHz typ.	YES	C14 B14	Not installed by default. 2.5V Diff Osc. may be purchased separately.

Table 6 – Available GCLK Sources

There are clocks on the board, which are included as reference for the Video DAC and Codec. These are 25.175MHz and 24.576MHz, respectively. These were not brought in on GCLK inputs and are connected to the FPGA via bus switches. JP20 must be present in order to use these clocks.

- Single-ended, 25.175MHz Oscillator / Header_IO(24) – FPGA pin "W21"
- Single-ended, 24.576MHz Oscillator / Header_IO(36) – FPGA pin "AE24"

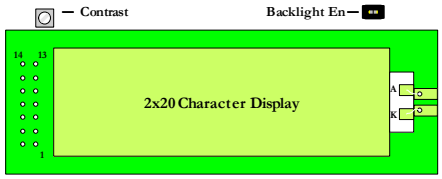
Freq	GCLK Input	FPGA pin#	Notes
25.175MHz	NO	W21	Use W/VGA. Shared with Header.
24.576MHz	NO	AE24	Use W/Codec. Shared with Header

Table 7 – Available Non-GCLK Osc.

2.5 On Board Displays (2x20 LCD & 128x64 OLED)

2.5.1 2x20 Character LCD

Manufacturer: Optrex
Part #: DMC-20261NYJ-LY-BCE



A 2x20 Character LCD is included with the Spartan-3 Development board. The displays LED backlight may be enabled using JP14. Contrast may be adjusted using potentiometer "R110". The display interface is either four or eight-bits wide, although our demos use the 8-bit option.

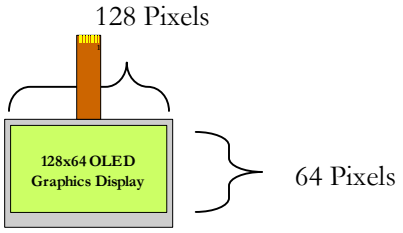
For detailed information, please see:
www.optrex.com/SiteImages/LitCentral/Dmcman_full.pdf

LCD Pin #	LCD Name	FPGA pin#
RS#	DISP_RS	P8
D0	DISP_D0	AE21
D1	DISP_D1	AF21
D2	DISP_D2	AE20
D3	DISP_D3	AF20
D4	DISP_D4	AE19
D5	DISP_D5	AE18
D6	DISP_D6	AE17
D7	DISP_D7	AD14
EN#	LCD_EN	R8

Table 8 – 2x20 Character LCD Pin-out

2.5.2 128x64 OSRAM Pictiva™ OLED Graphics Display

Manufacturer: OSRAM
Part #: OS128064PK16MY0A00



4-Bits/Pixel Single Color Graphics Display

The Spartan-3 Development board includes a 128x64 OSRAM Pictiva™ OLED(Organic Light Emitting Diode) graphics display. This is a 4-bit per pixel (grayscale) single-color passive matrix display. The display has a contrast ratio of 100:1 and a 160° viewing angle. The Pictiva displays are available in serial or parallel interface, although applications in this kit use the 8-bit parallel interface.

The parallel bus interface is compatible with 68-series and 80-series microcontrollers and is selectable at pin 4 of the ribbon cable (see pinout below). This will affect the function of several other pins as noted in the table below. The Spartan-3 Dev board uses a resistor jumper (JT5) to select the desired level of pin 4. By default the jumper is placed at pads 1-2 for a logic high enabling an 80-series interface. This placement is subject to change based on future demo applications.

Display Pin#	Pin Name	I/O	Description	FPGA Pin#
1	CS#	I	Chip Select – Active Low	AA4
2	RES#	I	Reset – Active Low	AA6
3	BS1	I	Interface Protocol Select. LOW = 68-series HIGH = 80-series	-
4	D/C#	I	Data / Command HIGH = Bus contains data for DDRAM LOW = Bus contains command	P8
5	R/W# (WR#)	I	Read/Write in 68 series mode Write strobe in 80-series mode	Y7
6	E (RD#)	I	E clock in 68-series mode Read strobe in 80-series mode	Y10
7	D0	I/O	Data 0	AE21
8	D1	I/O	Data 1	AF21
9	D2	I/O	Data 2	AE20
10	D3	I/O	Data 3	AF20
11	D4	I/O	Data 4	AE19
12	D5	I/O	Data 5	AE18
13	D6	I/O	Data 6	AE17
14	D7	I/O	Data 7	AD14
15	VSSB	I	n/c	-
16	VDD	I	Positive supply (2.4V – 3.5V)	-
17	VCC(VLL)	I	OLED Drive power (12V – 16V)	-
18	VSS	I	Ground	-

Table 9 - OLED Display Pin-out

The OLED drive voltage (VLL) must be between 12V and 16V. However, it requires very little operating current. Typical ILL is 20-24mA. So an on-board 12V supply could be used with little affect on the power budget. If there is no 12V supply

on board, one may design in a low-cost, low-power 12V source. The Spartan-3 Dev board uses a National Semiconductor LM2704 Micropower Step-up DC/DC Converter. This small (SOT23) converter has an input range of 2.2V-7V and an adjustable output up to 20V.

For more display information visit www.osram-os.com or www.pictiva.com.
For power supply information please see www.national.com.

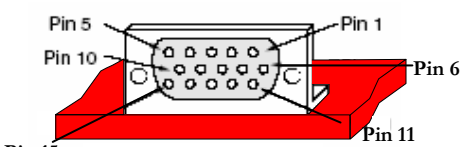
It should be noted that the 2x20 Character display and 128x64 graphics display share a common data bus. In designs where only one of the displays is to be used, the other's Enable (or CS) pin should be driven inactive using the FPGA. This will help avoid bus contention. An alternative is to simply remove the unused display from the board. The following table illustrates the pins which are common as well as the corresponding pin on the FPGA.

OLED Signal	LCD Name	FPGA pin#
DISP_CSB	-	AA4
DISP_RSTB	-	AA6
DISP_RS	DISP_RS	P8
DISP_RD_WRB	-	Y7
DISP_ECLK	-	Y10
DISP_D0	DISP_D0	AE21
DISP_D1	DISP_D1	AF21
DISP_D2	DISP_D2	AE20
DISP_D3	DISP_D3	AF20
DISP_D4	DISP_D4	AE19
DISP_D5	DISP_D5	AE18
DISP_D6	DISP_D6	AE17
DISP_D7	DISP_D7	AD14
-	LCD_EN	R8

Table 10 - OLED Display FPGA Pin-out

2.6 VGA (DB15 & Video DAC)

Manufacturer: Analog Devices
Part #: ADV7125KST140



DB15 VGA Connector

The Spartan-3 Development board provides a DB15 and Video DAC to drive an analog RGB monitor. RGB data is output from the FPGA in a 24-bit parallel format (8 bits each Red/Green/Blue). This data, along with clock, blanking and synchronization signals is provided to the ADV7125 triple video DAC for conversion to RS-343A/RS-170-compatible video signals to drive an RGB monitor. Note that the ADV7125 can accept 10-bit R, G and B data but pin utilization of the FPGA limits this data path to 24 instead of 30 bits. The eight R, G and B data bits are provided to the eight most-significant bits of the DAV7125 RGB inputs with the two least-significant bits of R, G and B held at ground level.

Also provided by the FPGA to the ADV7125 are composite synchronization and blanking signals. Vertical and horizontal synchronization signals are brought to pins 14 and 13 (respectively) of DB15 connector (P4) but are not required. The analog RGB signals generated by the ADV7123 are connected to P4 to drive an analog RGB monitor via a doubly terminated 75-ohm coaxial cable. The ADV7125 device internally encodes video synchronizing information onto the Green channel.

The 25.175MHz oscillator provides the required clocking for a 640 X 480 60Hz VGA monitor. This is determined as follows: horizontal lines (pixels) * vertical lines * refresh rate. Due to required overhead (e.g., horizontal and vertical retrace, etc), the 640 X 480 display is actually 800 X 525 (800 x 525 x 59.94 = 25.175e6). Note that while 60Hz is commonly used in discussion, the actual refresh rate is 59.94Hz. The oscillator may be replaced with a higher frequency oscillator to support higher resolution monitors; e.g., VGA (640 x 480) @72 Hz requires 31.5MHz, SVGA (800 x 600) @ 72Hz requires 50.0MHz, XGA (1024 X 768) @ 75 Hz requires 78.75MHz, SXGA (1280 X 1024) @ 75Hz requires 135.0MHz. The ADV7125KST140 140MHz device furnished on the board is sufficient for SXGA resolution at 75Hz.

Signal	*Header Equivalent Net	FPGA pin#
Red(0)	HDR_IO(0)	A19
Red(1)	HDR_IO(1)	A22
Red(2)	HDR_IO(2)	A20
Red(3)	HDR_IO(3)	A23
Red(4)	HDR_IO(4)	D19
Red(5)	HDR_IO(5)	A21
Red(6)	HDR_IO(6)	E19
Red(7)	HDR_IO(7)	B23
Green(0)	HDR_IO(8)	B22
Green(1)	HDR_IO(9)	C23
Green(2)	HDR_IO(10)	C22
Green(3)	HDR_IO(11)	B21
Green(4)	HDR_IO(12)	C21
Green(5)	HDR_IO(13)	E21
Green(6)	HDR_IO(14)	D21
Green(7)	HDR_IO(15)	F21
Blue(0)	HDR_IO(16)	E20
Blue(1)	HDR_IO(17)	B20
Blue(2)	HDR_IO(18)	F20
Blue(3)	HDR_IO(19)	D20
Blue(4)	HDR_IO(20)	F19
Blue(5)	HDR_IO(21)	B19
Blue(6)	HDR_IO(22)	G19
Blue(7)	HDR_IO(23)	C19
Video_clk	HDR_IO(24)	W21
Horiz_sync	HDR_IO(25)	W20
Vert_sync	HDR_IO(26)	Y21
Comp_sync	HDR_IO(27)	Y20
Blank	HDR_IO(28)	AC22

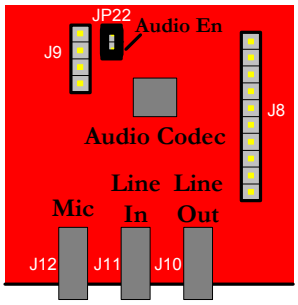
Table 11 – Video DAC - FPGA Pin-out

* Note: DAC signals are connected to the FPGA by way of a bus switch. This allows the re-use of header signals. If you wish to use the 50-pin header J17, you may disable the bus switches using JP20.

Jumper	Function	Default
JP23	On – disables oscillator U28	OFF
JP20	On – enables bus switches	ON
JT10	Resistor Jumper: 2-3 – Power save mode	1-2

Table 12 – Video DAC Jumpers

2.7 Audio Codec



Manufacturer: Philips
Part #: UCB1400BE

A Philips UCB1400 stereo 20-bitAudio CODEC is used to provide stereo line-level and monophonic microphone input and stereo line-level/headphone out functions for the Spartan-3 Development Board. 3.5mm audio jacks provide input/output connectivity as follows:

J10: Stereo line-level out
J11: Stereo line-level in
J12: Mono microphone in

The FPGA communicates with the UCB1400 via an AC97 interface. The UCB operates in master mode; with the FPGA operating as an AC97 controller device; in this mode the UCB1400 provides AC97 timing (Bit Clock). Details of the operation of the AC97 interface are somewhat complex and beyond the scope of this document. Refer to the UCB1400 data sheet and the AC97 Specification Rev. 2.1 for further details.

A 24.576MHz clock is provided to the UCB1400. This clock is also connected to the FPGA and may be disabled by placing a shunt at JP21.

2.7.1 Touch Panel Inputs

The UCB1400 includes a resistive touch panel controller that may be used to provide digitally encoded position data to the FPGA via the AC97 interface. X and Y touch screen inputs are provided to the UCB1400 via test points TP7, TP8, TP9, and TP10. An interrupt signal (IRQ_OUT) can be generated to the FPGA to indicate a touch panel entry was made.

2.7.2 General Purpose I/O & A/D Converter

The UCB1400 CODEC provides ten general-purpose I/O bits that may be set/read via the AC97 interface. Additionally, four analog voltage inputs may be multiplexed into the UCB1400's 10-bit A/D converter. The 10 GPIO bits are connected to Header J8 and the four analog voltages are input via Header J9.

Signal	*Header Equivalent Net	FPGA pin#
ac97_sdata_out	HDR_IO(29)	Y22
ac97_sdata_in	HDR_IO(30)	AD22
ac97_bit_clk	HDR_IO(31)	AB22
ac97_sync_out	HDR_IO(32)	AB23
ac97_reset_n	HDR_IO(33)	Y23
irq_out	HDR_IO(34)	AD23
adc_sync	HDR_IO(35)	AA23
clock_24_576M	HDR_IO(36)	AE24

Table 13 – Audio Codec - FPGA Pin-out

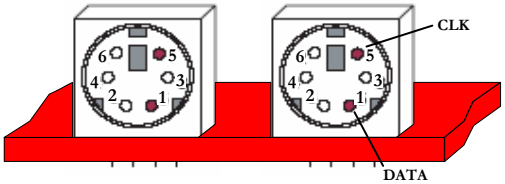
* Note: Codec signals are connected to the FPGA by way of a bus switch. This allows the re-use of header signals. If you wish to use the 50-pin header J17, you may disable the bus switches using JP20.

2.7.3 Codec Jumpers

Jumper	Function	Default
JP21	On – disables oscillator U26	OFF
JP20	On – enables bus switches	ON
JP22	On – Connects Reset to FPGA Off – Forces Codec into reset	ON

Table 14 – Audio Codec Jumpers

2.8 PS2 Keyboard & Mouse Ports



The Spartan-3 Dev Board includes two standard 6-pin Mini-Din (PS2) connectors labeled JS1 and JS2. This two-wire interface will provide connection to PS2 Mice or Keyboards. Since this is a two wire interface, only pins Data (pin-1) and Clk (pin-5) are connected to the FPGA. The following table provides the pinout for JS1 & JS2.

Pin	Function	*HDR Equivalent Net	FPGA Pin#
JS1 – pin 1	Data	HDR_IO(37)	AA24
JS1 – pin 5	CLK	HDR_IO(38)	AF24
JS2 – pin 1	Data	HDR_IO(39)	AB25
JS2 – pin 5	CLK	HDR_IO(40)	AB26

* Note: PS2 signals are connected to the FPGA by way of a bus switch (JP20 ON). This allows the re-use of header signals. If you wish to use the 50-pin header J17, you may disable the bus switches by removing JP20. Removing JP20 will disconnect the PS2 connectors from the FPGA.

PS2 Mouse/Keyboard protocol information may be found at:
http://panda.cs.ndsu.nodak.edu/~achapwes/PICmicro/PS2/ps2.htm

2.9 Dip & Push-Button Switches

An eight-position dipswitch (SPST) has been installed on the board and attached to the FPGA. These switches provide digital inputs to user logic as needed. The signals are pulled low (0) by 10K ohm resistors when the switch is open and tied to 2.5V (1) when the switch is closed.

Switch #	Signal Name	FPGA pin#
S1-1	SWITCH0	F1
S1-2	SWITCH1	F2
S1-3	SWITCH2	F3
S1-4	SWITCH3	G4
S1-5	SWITCH4	F4
S1-6	SWITCH5	G5
S1-7	SWITCH6	H6
S1-8	SWITCH7	H13

Table 15 - Dipswitch FPGA Pin-out

Two momentary closure push buttons have been installed on the board and attached to the FPGA. These buttons can be programmed by the user and are ideal for logic reset and similar functions. Pull down resistors hold the signals low (0) until the switch closure pulls it high (1).

Silkscreen Part #	Signal Name	FPGA pin#
SW2	SWITCH_PB1	H14
SW3	SWITCH_PB2	H15

Table 16 - Pushbutton FPGA Pin-out

2.10 LEDs

Eight discrete LEDs are installed on the board and can be used to display the status of the internal logic. These LEDs are attached as shown below and are lit by forcing the associated FPGA I/O pin to a logic (1) and are off when the pin is either Low (0) or not driven.

LED #	Signal Name	FPGA pin#
D1	LED0	U4
D2	LED1	W4
D3	LED2	V6
D4	LED3	W7
D5	LED4	T8
D6	LED5	T7
D7	LED6	T6
D8	LED7	T5

Table 17 - LED FPGA Pin-out

2.11 Piezo Buzzer

The Spartan-3 Development board includes a piezo buzzer that may be used to generate simple audio tones. To enable the buzzer, install a jumper at JP30 and JP20 (both installed by default). Drive the buzzer with an oscillating signal at pin AD25.

2.12 High-speed Serial Communication

2.12.1 LVDS

The Spartan-3 Development board uses one of the AvBus connectors (P2) to provide up to 30 LVDS pairs. These pairs, labeled LVDS_P(0:29) and LVDS_N(0:29) are matched length. Each pair _P and _N are routed as differential pairs and are tightly coupled. Each pair may be used as transmit or receive and should be configured accordingly using termination resistors at the provided surface-mount pads. By default, no termination resistors are installed. A resistor should be added for each of the receive pairs (see schematic sheet 14).

LVDS Signal	Net Length(mm)	Term Resistor	P2 Pin #	FPGA pin#
LVDS_P0	95.33915	R118	3	E24
LVDS_N0	95.26315		2	E23
LVDS_P1	95.02096	R119	74	F24
LVDS_N1	95.74285		73	F23
LVDS_P2	95.12807	R120	77	G23
LVDS_N2	95.84996		76	G22
LVDS_P3	95.6622	R121	9	E26
LVDS_N3	95.5862		8	E25
LVDS_P4	95.07538	R122	80	H21
LVDS_N4	95.79727		79	H20
LVDS_P5	95.16827	R123	83	J23
LVDS_N5	95.89016		82	J22
LVDS_P6	95.51224	R124	15	G21
LVDS_N6	95.43624		14	G20
LVDS_P7	95.13984	R125	86	K26
LVDS_N7	95.86173		85	K25
LVDS_P8	95.04799	R126	18	G26
LVDS_N8	95.61788		17	G25
LVDS_P9	95.17269	R127	21	H26
LVDS_N9	95.74258		20	H25
LVDS_P10	95.56244	R128	92	M22
LVDS_N10	95.63844		91	M12
LVDS_P11	95.1024	R129	24	K24
LVDS_N11	95.0264		23	K23
LVDS_P12	95.06954	R130	95	N22
LVDS_N12	95.80315		94	N21
LVDS_P13	95.71661	R131	27	L26
LVDS_N13	95.64061		26	L25
LVDS_P14	95.53837	R132	33	M20
LVDS_N14	95.46237		32	M19
LVDS_P15	95.94724	R133	104	P19
LVDS_N15	95.16314		103	P20
LVDS_P16	95.79405	R134	110	R21
LVDS_N16	95.24426		109	R22
LVDS_P17	95.15417	R135	42	N24

LVDS_N17	95.72406		41	N23
LVDS_P18	95.93547	R136	113	T21
LVDS_N18	95.3271		112	T22
LVDS_P19	95.80103	R137	45	P21
LVDS_N19	95.04219		44	P22
LVDS_P20	95.85368	R138	116	U23
LVDS_N20	95.19809		115	U24
LVDS_P21	95.96422	R139	48	T25
LVDS_N21	95.27415		47	T26
LVDS_P22	95.80083	R140	51	U25
LVDS_N22	95.09904		50	U26
LVDS_P23	95.86594	R141	122	W25
LVDS_N23	95.2591		121	W26
LVDS_P24	95.95932	R142	54	V24
LVDS_N24	95.03457		53	V25
LVDS_P25	95.93609	R143	125	R19
LVDS_N25	95.03483		124	R20
LVDS_P26	95.97747	R144	57	V22
LVDS_N26	95.21863		56	V23
LVDS_P27	95.93873	R145	128	T19
LVDS_N27	95.33188		127	T20
LVDS_P28	95.81595	R146	60	Y25
LVDS_N28	95.05711		59	Y26
LVDS_P29	95.94143	R147	63	AC25
LVDS_N29	95.18259		62	AC26

Table 18 - LVDS FPGA Pin-out

2.13 Memory

The Spartan-3 Development board is populated with 32MB DDR SDRAM, 16MB Flash, and 2MB SRAM. Additional memory including Flash, SDRAM, and SRAM are available with the purchase of the Avnet Communications/Memory Module.

2.13.1 DDR SDRAM

Manufacturer: Micron
Part #: MT46V16M16

One Micron DDR SDRAM device, part number: MT46V16M16-4, provides a 16-bit data bus.

Attributes of the DDR SDRAM on the Spartan-3 Development board:

- 32MB (one 16 Meg x 16 device)
- 60-ball FBGA (16mm x 9mm)
- Board supplies 2.5V to VDD and VDDQ
- 6ns access time (CL = 2 @ 133 MHz, CL = 2.5 @ 333 MHz)

The following table lists the timing parameters required to set up the SDRAM peripheral in EDK for 100 MHz operation (parameters are entered in the MHS file). If a timing parameter is left out of the peripheral instantiation, a default value is automatically used. The Software/BSP section of this manual has more information about setting up peripherals in EDK.

PLB DDRperipheral – Timing Parameter	Time (ps) or Number
C_DDR_TMRD	12000
C_DDR_TWR	15000
C_DDR_TWTR	1
C_DDR_TRAS	70000
C_DDR_TRC	60000
C_DDR_TRFC	72000
C_DDR_TRCD	18000
C_DDR_TRRD	12000
C_DDR_TRP	18000
C_DDR_TREFI	7800000
C_DDR_CAS_LAT	2
C_DDR_DWIDTH	32
C_DDR_AWIDTH	13
C_DDR_COL_AWIDTH	9
C_DDR_BANK_AWIDTH	2
C_PLB_CLK_PERIOD_PS	10000

Table 19 - Timing Parameters for DDR SDRAM Peripheral

2.13.2 Flash

Manufacturer: Intel
Part #: TE28F640J3C120

Two 64 Mbit devices, 4M x 16, make up the 32-bit Flash data bus. The devices have an operating voltage of 3.3V and provide 16 MB total of Flash memory. The Flash is connected to the Spartan-3 FPGA via a shared memory bus that also services the SRAM and one AvBus connector (P3).

An example project, using the OPB_EMC is included with the Spartan-3 Dev kit. This example will provide correct timing parameters for operating the SRAM and Flash devices. See the Software/BSP section of this manual for more information.

2.13.3 SRAM

Manufacturer: Cypress
Part #: CY7C1062AV33-12BGC

A single Cypress Asynchronous SRAM device, part number: CY7C1062AV33-12BGC, connects to the 32-bit wide shared data bus. The Cypress device provides 2 MB of SRAM memory on a single IC and is organized as 512K x 32. The device has an operating voltage of 3.3V and a –12 speed grade for 80 MHz operation.

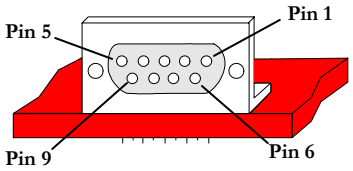
An example project, using the OPB_EMC is included with the Spartan-3 Dev kit. This example will provide correct timing parameters for operating the SRAM and Flash devices. See the Software/BSP section of this manual for more information.

2.14 Communication (RS232, 10/100 Ethernet, USB2.0)

For communication, the Spartan-3 FPGA has access to an RS232 transceiver, a 10/100 Ethernet PHY, and a USB2.0 transceiver.

2.14.1 RS232

Manufacturer: Harris/Intersil
Part #: ICL3222CA



DB9 Serial Connector

The RS232 transceiver is a 3222 available from Harris/Intersil (ICL3222CA) and Analog Devices (ADM3222). This transceiver is operating at 3.3V for VCC. The FPGA transmit/receive signals are connected to a 2.5V I/O bank of the FPGA (Bank 6). Because the 3222 minimum logic threshold high is 2V, the 2.5V bank will work for this interface. The internal charge pump creates the RS232 compatible output levels.

The standard RX and TX lines (pin3 and pin2) are connected to the FPGA by way of the 3222. The RTS/CTS pins may be jumpered out, allowing the FPGA pins to be directly connected to the USB IC's RS232 port. The FPGA will be connected to RTS/CTS when jumpers JP28 and JP29 are at position 1-2. Otherwise, in position 2-3, the FPGA will not be connected to RTS/CTS, but to the RS232 RX/TX lines of the USB IC.

A straight through serial cable should be used to plug "J3" into a standard PC serial port (male DB9).

Signal Name	FPGA pin#	Xcvr pin#
Transmit (RS232_TX1)	P5	13
Receive (RS232_ RX1)	P4	15
*CTS (RS232_ CTS)	P7	12
*RTS (RS232_ RTS)	P6	10

Table 20 - RS232 FPGA Pin-out

Signal Name	DB9 J3	Xcvr pin#
TX	2	17
RX	3	16
CTS	8	8
RTS	7	9
GND	5	-

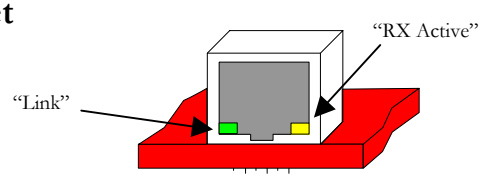
Table 21 - RS232 Connector Pin-out

* Note: RTS and CTS are only connected to the FPGA when JP28 and JP29 are in position 1-2.

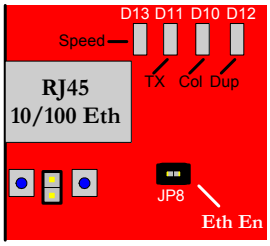
2.14.2 10/100 Ethernet

Transceiver –
Manufacturer: National Semiconductor
Part #: DP83847ALQA56A

Connector –
Manufacturer: Pulse
Part #: J0026D01B



RJ45 Ethernet Connector



The on-board Ethernet PHY is a National DP83847ALQA56A DsPHYTER® II. The DP83847 is a small, low power physical layer transceiver that only requires a single 3.3V supply. The PHY supports 3.3V signaling levels to the MAC interface, in this case the Spartan-3 FPGA. The PHY is connected to a Pulse RJ-45 jack with integrated magnetics (part number: J0026D01B). The jack also integrates two LEDs to show Link and Receive Activity. Four more LEDs are provided on the board for status indication. These LEDs indicate Link Speed (D13), Transmit Activity (D11), Collision Detect (D10) and Full Duplex operation (D12). The PHY clock is generated from its own 25 MHz crystal. The PHY address is set to binary "00011". Three-pad resistor jumpers were used to set the operating mode (JT1, JT2 and JT3). An illustration of the resistor jumper footprint is shown below.

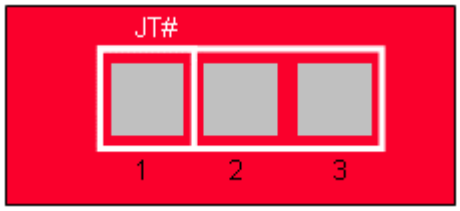


Figure 17 - Resistor Jumper Pin-out

These jumper pads provide the user with the ability to change the operating mode by moving the resistors. By default the PHY is set to auto negotiate a link with a peer. The available modes of operation are shown in the table below.

Operating Modes	JT3	JT2	JT1
10BaseT Half Duplex, Forced Mode	2-3	2-3	2-3
10BaseT Full Duplex, Forced Mode	2-3	2-3	1-2
100Base-TX Half Duplex, Forced Mode	2-3	1-2	2-3
100Base-TX Full Duplex, Forced Mode	2-3	1-2	1-2
10BaseT Half/Full Duplex Advertised, Auto-negotiate	1-2	2-3	2-3
100Base-TX Half/Full Duplex Advertised, Auto-negotiate	1-2	2-3	1-2
10BaseT/100Base-TX Half Duplex Advertised, Auto-negotiate	1-2	1-2	2-3
10BaseT/100Base-TX Half/Full Duplex, Auto-negotiate (Default)	1-2	1-2	1-2

Table 22 - Ethernet PHY Modes

Reference Designator	Function	Note
JP8	Ethernet Enable	Installed by default
JT1-3	Operating Mode	Resistor Jumpers (see table above)
D10	Collision Detect	
D11	TX Activity	
D12	Duplex	
D13	Speed Indicator	

Table 23 - Ethernet Jumpers and LEDs

The use of this port requires an Ethernet MAC core to be instantiated in the FPGA project. The example project that includes network support utilizes a licensed IP core from Xilinx. A valid license for this IP may be required to regenerate the project. The following table provides the FPGA pin numbers for the Ethernet PHY interface.

Signal Name	FPGA pin#		Signal Name	FPGA pin#
MII_MDC	P2		MII_CRS	AA1
MII_MDIO	P1		MII_COL	AA2
MII_TXD0	W1		MII_RXD0	R3
MII_TXD1	W2		MII_RXD1	R2
MII_TXD2	Y1		MII_RXD2	R1
MII_TXD3	Y2		MII_RXD3	P3
MII_TXEN	V2		MII_RXDV	T1
MII_TXERR	U2		MII_RXERR	U1
MII_TX_CLK	U3		MII_RXCLK	T2

Table 24 - Ethernet FPGA Pin-out

For DP83847 literature, please see:
www.national.com/pf/DP/DP83847.html

For more information on National Semiconductor Ethernet products, please see:
www.national.com/appinfo/networks/

For information on connector offerings from Pulse, please see:
www.pulseeng.com

2.14.3 USB 2.0

Manufacturer: Cypress
Part #: CY7C68013-100AC

The Spartan-3 Development Board includes a Cypress EZ-USB FX2™ USB Microcontroller, part number CY7C68013-100AC. The EZ-USB FX2 device is a single-chip integrated USB 2.0 transceiver, Serial Interface Engine (SIE) and 8051 microcontroller. This device supports full-speed (12 Mbps) and high-speed (480 Mbps) modes, but does not support low-speed mode (1.5 Mbps). The FX2 interface to the Spartan-3 FPGA is a programmable state machine that supports 8- or 16-bit parallel data transfers. This interface is called the General Programmable Interface (GPIF). The GPIF is controlled by Waveform Descriptors that are created with the Cypress "GPIFTool" utility and downloaded to the FX2 over the USB cable. The GPIF descriptors are stored in internal RAM and are loaded by the firmware during initialization. The GPIF interface is made up of the signals in the following table, which are connected to Spartan-3 FPGA. Some of the additional GPIF pins are connected to the SelectMAP configuration port on the Spartan-3 FPGA. This provides for the development of a FPGA configuration tool, which may be created by Avnet at a later date. The additional pins used for the SelectMAP interface are shaded in the following table.

The USB FX2 device can also be used in a slave mode where the FPGA accesses the FX2 like a FIFO. For more information about the FX2 modes of operation, see the "EZ-USB FX2 Technical Reference Manual" and the FX2 datasheet available on Cypress Semiconductor's web site (http://www.cypress.com).

FX2 Signal	FPGA net	FPGA pin	Description
CTL[0]	USB_CTL0	AD2	Programmable control outputs
CTL[1]	USB_CTL1	AD1	
CTL[2]	USB_CTL2	AC2	
CTL[3]	CTL3_PROG#		Output enable for FPGA_PROG# driver
CTL[4]	FPGA_CS#		SelectMAP port chip select
CTL[5]	FPGA_RDWR#		SelectMAP port read/write enable
RDY[0]	USB_RDY0	W3	Sample-able ready inputs
RDY[1]	USB_RDY1	W6	
RDY[2]	FPGA_BUSY		SelectMAP port busy indication
RDY[3]	FPGA_DONE		FPGA configuration DONE pin
RDY[4]	FPGA_INIT#		FPGA initialization pin
RDY[5]	USB_RDY5		Sample-able ready input connected to JP6:15
FD[0]	USB_FD0 (D0)	Y15	Bidirectional FIFO data bus (also SMAP data)
FD[1]	USB_FD1 (D1)	W14	
FD[2]	USB_FD2 (D2)	Y14	
FD[3]	USB_FD3 (D3)	AA14	
FD[4]	USB_FD4 (D4)	AC13	
FD[5]	USB_FD5 (D5)	AB13	
FD[6]	USB_FD6 (D6)	AB12	
FD[7]	USB_FD7 (D7)	AA12	
FD[8]	USB_FD8	W5	Bidirectional FIFO data bus
FD[9]	USB_FD9	R5	
FD[10]	USB_FD10	U7	
FD[11]	USB_FD11	T4	
FD[12]	USB_FD12	V7	
FD[13]	USB_FD13	V5	
FD[14]	USB_FD14	V4	
FD[15]	USB_FD15	V3	
GPIFADR[0]	USB_PC0		Optional FPGA_CCLK out – see JT5 selection
GPIFADR[1]	FPGA_M2		SelectMAP port mode - M2
GPIFADR[2]	FPGA_M1		SelectMAP port mode - M1
GPIFADR[3]	FPGA_M0		SelectMAP port mode - M0
GPIFADR[4]	JTAG_TDI		Optional JTAG interface – TDI (install RP96)
GPIFADR[5]	JTAG_TDO		Optional JTAG interface – TDO (install RP96)
GPIFADR[6]	JTAG_TMS		Optional JTAG interface – TMS (install RP96)
GPIFADR[7]	JTAG_TCK		Optional JTAG interface – TCK (install RP96)
GPIFADR[8]	USB_PE7		Address output connected to JP6:16
IFCLK	USB_IFCLK	U5	Interface clock, optional FPGA_CCLK (JT5)
PA0/INT0#	USB_INT0#	AC1	Port A I/O or active-low interrupt 0
PA1/INT1#	USB_INT1#	AB4	Port A I/O or active-low interrupt 1
PA2/SLOE	USB_SLOE	AB3	Port A I/O or slave-FIFO output enable
*PA3/WU2	*USB_WU2	*AA5	Port A I/O or alternate wake-up pin
PA4/FIFOADR0	USB_FA0	AA3	Port A I/O or slave-FIFO address select 0
PA5/FIFOADR1	USB_FA1	Y6	Port A I/O or slave-FIFO address select 1
PA6/PKTEND	USB_PEND	Y5	Port A I/O or slave-FIFO packet end
PA7/SLCS#	USB_SLCS#	Y4	Port A I/O or slave-FIFO enable
RESET#	RST#	R6	USB device active-low reset

Table 25 - USB Interface FPGA Pin-out

* Only connected on 3S2000 device. 1500 is a no-connect.

2.15 I/O Connectors

The Spartan-3 Development board is an Avnet Avenue Solutions compliant motherboard that incorporates board-to-board connectors to support Avalon expansion boards. The connection between the Spartan-3 Development board and the Avnet Avenue Solutions compliant daughter boards is via the Avnet standard AvBus connectors (P1, P2, J14 and J15). The connectors on the top side of the evaluation board (P1, P2) are the host connectors, AMP part number 179031-6. The host connectors mate with AMP part number 5-179010-6. Connectors on the bottom side (J14, J15) are AMP part number 5-179010-6. Since the Spartan-3 Development is intended as a host, the bottom (solder side) connectors (J14, J15) are not populated by default.

2.15.1 AvBus Connectors

The Spartan-3 FPGA is connected to two mirrored 140-pin board-to-board AvBus standard connectors. This means that each signal connected to P1 is mirrored on the opposite side of the board by the same pin number on J14. Similarly, P2 is mirrored by J15.

AvBus "P1"

The AvBus connector labeled "P1" is directly connected to 88 I/O of the Spartan-3. These signals, labeled AV_D(0:31), AV_A(0:31), and AV_CTL(0:23) are connected to voltage selectable banks 0 and 1 of the FPGA.

AvBus "P2"

The AvBus connector labeled "P2" is directly connected to 93 I/O of the Spartan-3. These signals, labeled GEN_IO(0:32), LVDS_N(0:29), and LVDS_P(0:29) are connected to voltage selectable banks 2 and 3 of the FPGA. Note that the signals labeled LVDS are routed as differential pairs. This means that, for example, LVDS_N(0) is tightly coupled with LVDS_P(0). Consequently, any LVDS signal left floating will experience cross-talk from it's counterpart signal. This should be taken into account by the user when developing custom expansion cards.

AvBus "J14"

The AvBus connector labeled "J14" is a mirror of "P1". All signals are connected, pin-to-pin with P1. The only exceptions are the JTAG signals. This connector is not populated by default since the Spartan-3 Dev is intended to be the host.

AvBus "J15"

The AvBus connector labeled "J15" is a mirror of "P2". All signals are connected, pin-to-pin with P2. This connector is not populated by default since the Spartan-3 Dev is intended to be the host.

2.15.2 Header "JP1"

The 50-pin header labeled "J17" on the Spartan-3 Development board is connected to 47 I/O pins on the Spartan-3 FPGA. Pin 48 on the header provides either 3.3V or 5.0V depending on the jumper pad installation on JT9 (3.3V is the default). Note that the pins of header JP1 are shared with several other peripherals including Video DAC, Audio Codec, PS2, and buzzer by way of bus switches. The bus switches may be disabled by removing JP20. Doing so will isolate the header from the extra peripherals, leaving only the header connected directly to the FPGA.

The tables on the following pages show pin-outs for the header and AvBus connectors.

Name	FPGA PIN #	Connector PIN #			FPGA PIN #	Name
AV_A0	B3	71		1	-	+5VDC
GND	-	72		2	A3	AV_A1
AV_A3	E6	73		3	A4	AV_A2
AV_A4	B4	74		4	-	GND
GND	-	75		5	D6	AV_A5
AV_A7	F7	76		6	C4	AV_A6
AV_A8	A5	77		7	-	GND
+3.3VDC	-	78		8	E7	AV_A9
AV_A11	F8	79		9	B5	AV_A10
AV_A12	C5	80		10	-	GND
GND	-	81		11	D8	AV_A13
AV_A15	G8	82		12	A6	AV_A14
AV_A16	B6	83		13	-	+5VDC
GND	-	84		14	E8	AV_A17
AV_A19	F9	85		15	C6	AV_A18
AV_A20	A7	86		16	-	GND
GND	-	87		17	D9	AV_A21
AV_A23	G9	88		18	B7	AV_A22
AV_A24	D7	89		19	-	GND
+3.3VDC	-	90		20	E9	AV_A25
AV_A27*	F10	91		21	A8	AV_A26
AV_A28*	B8	92		22	-	GND
GND	-	93		23	D10	AV_A29*
AV_A31	G10	94		24	C8	AV_A30*
AV_D0	B9	95		25	-	+5VDC
GND	-	96		26	E10	AV_D1
AV_D3	G11	97		27	C9	AV_D2
AV_D4	A10	98		28	-	GND
GND	-	99		29	E11	AV_D5
AV_D7	H11	100		30	B10	AV_D6
AV_D8	C10	101		31	-	GND
+3.3VDC	-	102		32	F11	AV_D9
AV_D11	G12	103		33	A11	AV_D10
AV_D12	B11	104		34	-	GND
GND	-	105		35	E12	AV_D13
AV_D15	H12	106		36	D11	AV_D14
AV_D16	A12	107		37	-	+5VDC
GND	-	108		38	F12	AV_D17
AV_D19	F13	109		39	B12	AV_D18
AV_D20	C12	110		40	-	GND
GND	-	111		41	D13	AV_D21
AV_D23	G13	112		42	B13	AV_D22
AV_D24	C13	113		43	-	GND
+3.3VDC	-	114		44	E13	AV_D25
AV_D27	F14	115		45	E14	AV_D26
AV_D28	D14	116		46	-	GND
GND	-	117		47	A14	AV_D29
AV_D31	G14	118		48	C15	AV_D30
AV_CTL0	B15	119		49	-	+5VDC
GND	-	120		50	E15	AV_CTL1
AV_CTL3	G15	121		51	A15	AV_CTL2
AV_CTL4	D16	122		52	-	GND
GND	-	123		53	F15	AV_CTL5
AV_CTL7	F16	124		54	B16	AV_CTL6
AV_CTL8	A16	125		55	-	GND
+3.3VDC	-	126		56	E16	AV_CTL9
AV_CTL11	G16	127		57	C17	AV_CTL10
AV_CTL12	B17	128		58	-	GND
GND	-	129		59	D17	AV_CTL13
AV_CTL15	F17	130		60	A17	AV_CTL14
AV_CTL16	C18	131		61	-	+5VDC
GND	-	132		62	E17	AV_CTL17
AV_CTL19	G17	133		63	B18	AV_CTL18
AV_CTL20	D18	134		64	-	GND
GND	-	135		65	F18	AV_CTL21
AV_CTL23*	G18	136		66	E18	AV_CTL22*
AVBUS_TMS	-	137		67	-	GND
+3.3VDC	-	138		68	-	AVBUS_TDO
AVBUS_TDI	-	139		69	-	AVBUS_TCK
JTAG_TRST#	-	140		70	-	GND

Table 26 - AvBus Connector "P1" Pin-out

Name	FPGA PIN #	Connector PIN #			FPGA PIN #	Name
GEN_IO0	D26	71		1	-	+5VDC
GND	-	72		2	E23	LVDS_N0
LVDS_N1	F23	73		3	E24	LVDS_P0
LVDS_P1	F24	74		4	-	GND
GND	-	75		5	J20	GEN_IO1
LVDS_N2	G22	76		6	F26	GEN_IO2
LVDS_P2	G23	77		7	-	GND
+3.3VDC	-	78		8	E25	LVDS_N3
LVDS_N4	H20	79		9	E26	LVDS_P3
LVDS_P4	H21	80		10	-	GND
GND	-	81		11	H22	GEN_IO3
LVDS_N5	J22	82		12	J21	GEN_IO4
LVDS_P5	J23	83		13	-	+5VDC
GND	-	84		14	G20	LVDS_N6
LVDS_N7	K25	85		15	G21	LVDS_P6
LVDS_P7	K26	86		16	-	GND
GND	-	87		17	G25	LVDS_N8
GEN_IO5	H23	88		18	G26	LVDS_P8
GEN_IO6	K20	89		19	-	GND
+3.3VDC	-	90		20	H25	LVDS_N9
LVDS_N10	M21	91		21	H26	LVDS_P9
LVDS_P10	M22	92		22	-	GND
GND	-	93		23	K23	LVDS_N11
LVDS_N12	N21	94		24	K24	LVDS_P11
LVDS_P12	N22	95		25	-	+5VDC
GND	-	96		26	L25	LVDS_N13
GEN_IO7	J24	97		27	L26	LVDS_P13
GEN_IO8	J25	98		28	-	GND
GND	-	99		29	K22	GEN_IO9
GEN_IO11	L22	100		30	L23	GEN_IO10
GEN_IO12	L21	101		31	-	GND
+3.3VDC	-	102		32	M19	LVDS_N14
LVDS_N15	P20	103		33	M20	LVDS_P14
LVDS_P15	P19	104		34	-	GND
GND	-	105		35	L20	GEN_IO13
GEN_IO15	M24	106		36	M26	GEN_IO14
GEN_IO16	L29	107		37	-	+5VDC
GND	-	108		38	N25	GEN_IO17
LVDS_N16	R22	109		39	N20	GEN_IO18
LVDS_P16	R21	110		40	-	GND
GND	-	111		41	N23	LVDS_N17
LVDS_N18	T22	112		42	N24	LVDS_P17
LVDS_P18	T21	113		43	-	GND
+3.3VDC	-	114		44	P22	LVDS_N19
LVDS_N20	U24	115		45	P21	LVDS_P19
LVDS_P20	U23	116		46	-	GND
GND	-	117		47	T26	LVDS_N21
GEN_IO19	N19	118		48	T25	LVDS_P21
GEN_IO20	P25	119		49	-	+5VDC
GND	-	120		50	U26	LVDS_N22
LVDS_N23	W26	121		51	U25	LVDS_P22
LVDS_P23	W25	122		52	-	GND
GND	-	123		53	V25	LVDS_N24
LVDS_N25	R20	124		54	V24	LVDS_P24
LVDS_P25	R19	125		55	-	GND
+3.3VDC	-	126		56	V23	LVDS_N26
LVDS_N27	T20	127		57	V22	LVDS_P26
LVDS_P27	T19	128		58	-	GND
GND	-	129		59	Y26	LVDS_N28
GEN_IO21	P24	130		60	Y25	LVDS_P28
GEN_IO22	P23	131		61	-	+5VDC
GND	-	132		62	AC26	LVDS_N29
GEN_IO23	R26	133		63	AC25	LVDS_P29
GEN_IO24	R24	134		64	-	GND
GND	-	135		65	T23	GEN_IO25
GEN_IO27	U22	136		66	U20	GEN_IO26
GEN_IO28	V21	137		67	-	GND
+3.3VDC	-	138		68	V20	GEN_IO29
GEN_IO31	W24	139		69	W22	GEN_IO30
GEN_IO32	AA26	140		70	-	GND

Table 27 - AvBus Connector "P2" Pin-out

JP1: Header 25x2					
Pin	FPGA	Signal	Signal	FPGA	Pin
1	A19	HDR_IO0	HDR_IO1	A22	2
3	A20	HDR_IO2	HDR_IO3	A23	4
5	D19	HDR_IO4	HDR_IO5	A21	6
7	E19	HDR_IO6	HDR_IO7	B23	8
9	B22	HDR_IO8	HDR_IO9	C23	10
11	C22	HDR_IO10	HDR_IO11	B21	12
13	C21	HDR_IO12	HDR_IO13	E21	14
15	D21	HDR_IO14	HDR_IO15	F21	16
17	E20	HDR_IO16	HDR_IO17	B20	18
19	F20	HDR_IO18	HDR_IO19	D20	20
21	F19	HDR_IO20	HDR_IO21	B19	22
23	G19	HDR_IO22	HDR_IO23	C19	24
25	W21	HDR_IO24	HDR_IO25	W20	26
27	Y21	HDR_IO26	HDR_IO27	Y20	28
29	AC22	HDR_IO28	HDR_IO29	Y22	30
31	AD22	HDR_IO30	HDR_IO31	AB22	32
33	AB23	HDR_IO32	HDR_IO33	Y23	34
35	AD23	HDR_IO34	HDR_IO35	AA23	36
37	AE24	HDR_IO36	HDR_IO37	AA24	38
39	AF24	HDR_IO38	HDR_IO39	AB25	40
41	AB26	HDR_IO40	HDR_IO41	AD25	42
43	AE22	HDR_IO42	HDR_IO43	AE23	44
45	AF22	HDR_IO44	HDR_IO45	AF23	46
47	AF14	CLK_HDR	3.3V/5.0V	-	48
49	-	Ground	Ground	-	50

Table 28 - Header "JP1" Pin-out

2.16 Power

The Spartan-3 Development Kit includes a 5V AC/DC Adapter that plugs into the board at "J7".
The Spartan-3 Development board uses a 5V AC/DC adapter (supplied with the kit) with center positive barrel connector. The 5V is used as the input to a TI PT6944A that provides 3.3VDC and 1.2VDC. Two National Semiconductor LP3966-ADJ parts provide 2.5V and 1.8V. A separate DDR Termination Regulator (National LP2995) is used to provide 1.25V reference and termination voltages. A National LM2704 is used to provide +12V to the OLED display. The barrel connector "J7" is shown below in Figure 18.

IMPORTANT:
Note that there is **no protection for reverse power supply polarity** so take necessary precautions to ensure that the center pin is 4.5V – 5.5V, and the ring is ground!

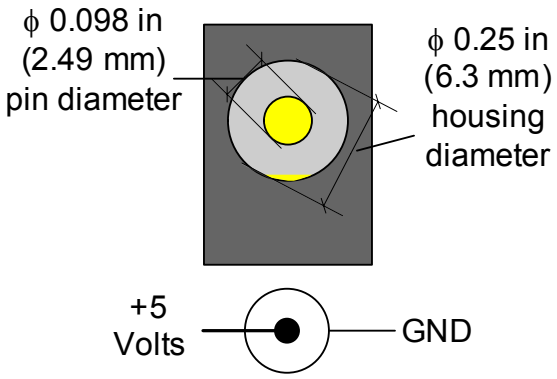


Figure 18 - Barrel Power Connector "J7"

3.0 Software/BSP

This section of the manual describes the example EDK projects included in the kit.

3.1 What is included

All of the example projects included in the Spartan-3 Development Kit were created in the Xilinx Embedded Development Kit (EDK) version 6.3. The examples include the Xilinx Platform Studio (XPS) project files and supporting directory structures; all of the required files to run the XPS projects. The user must have both the Xilinx Integrated Software Environment (ISE) version 6.3 and the EDK version 6.3 software installed to utilize the example projects. The following list provides an outline of the Board Support Package section. The XPS example projects are included on the Spartan-3 Development Kit CD. With the exception of the webserver example, each project will have a datasheet located at the project root directory. The webserver example is based on an app note from Xilinx (XAPP433).

- **XPS Example Projects**
  - **Hello World**
  - **Memory Examples**
  - **TBD**

3.2 Hello World

This example is intended to be as simple as possible in order to introduce the user to the board and Xilinx Platform Studio (XPS) tools. The design consists primarily of the processor and a uart that is set up as the standard I/O device. This will allow any print commands to be displayed on a terminal interface.

Since the design was built as a top-level system, the entire tool flow is within the XPS environment. The user may generate a netlist for the hardware system, compile the test software and create a bit file updated with the software all from within XPS. The user may even download the bit file to the evaluation board from XPS using a download cable. See Section 2.2 for instructions on how to set up a download cable for configuration. The user can make a change to the software, re-compile and re-generate a bit file without having to run through synthesis and implementation over again. To do this, select "Compile Program Sources" and then "Update Bitstream". Finally just download the bit file to the board using the "Download" option.

3.3 On-Chip Peripheral Bus (OPB) External Memory Project(s)

These are currently to be determined. Likely projects will include DDR SDRAM, Flash and SRAM.

3.3.1 DDR SDRAM Project

This example uses the On-Chip Peripheral Bus (OPB) to interface with the OPB_DDR peripheral, which is a standard peripheral included in the EDK. The peripheral handles all transactions between the OPB and the off-chip DDR SDRAM memory, allowing the MicroBlaze access to the 32MB memory. The timing parameters of the SDRAM peripheral have been specifically set up for the Micron DDR SDRAM device on the Spartan-3 Development board. The OPB clock frequency is set for 100 MHz, since the 100MHz oscillator input is being used. The timing parameters stay the same for the DDR SDRAM regardless of the bus frequency. The peripheral automatically generates the specified timing using the specified bus frequency.

3.3.2 SRAM / Flash Project

This example uses the On-Chip Peripheral Bus (OPB) to interface with the OPB_EMC (External Memory Controller) peripheral, which is a standard peripheral included in the EDK. The peripheral handles all transactions between the OPB and the off-chip SRAM and Flash memory, allowing the MicroBlaze access to the 16MB Flash and 2MB SRAM. The timing parameters of the Flash and SRAM peripheral have been specifically set up for the Intel and Cypress devices on the Spartan-3 Development board.

3.4 Web Server

The Web Server demo is based on a Xilinx application note XAPP 433 that uses the MicroBlaze soft processor and the OPB Ethernet MAC peripheral to host a web page. The original application note and accompanying source files are available here: http://direct.xilinx.com/bvdocs/appnotes/xapp433.pdf. The complete XPS project is included on the Spartan-3 Development Kit CD under the "demo" folder. Since this design is documented in the application note, the only additional documentation is a readme file in the root directory of the project. This "avnet_readme.txt" file discusses the modifications made during the port to the Avnet Spartan-3 Development Board and provides instructions on how to run the demo.

4.0 List of Partners